NOVATEK
聯 詠 科 技

Data Sheet

NT3916

One-chip Driver IC with internal GRAM
for 262,144 colors 176 RGB x 220 dot TFT LCD

Version 1.0.1
2006/11/17

ABBREVIATIONS AND VOCABULARY

↑	Rising edge active
/CSX	Chip Select, active low
AM	Active Matrix
AGND	Analog ground
ASIC	Application Specific Integrated Circuit
AV	Audio-Visual Entities
AVDD	Source driver supply voltage (Driver internal analog supply voltage)
B/W	Black & White
COG	Chip On Glass
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
D/CX	Display Data/Command data select, Command data is active low
DE	Date Enable
DGND	Digital (Logic) ground
DIN	Data In, display side
DOUT	Data Out, display side
E	Read and Write Function in 6800 MCU I/F
EMR	Electro Magnetic Resonance
EMC	Electro Magnetic Compatibility
fps	Frame per second
FPWB	Flexible Printed Wiring Board
Hi-Z	High Impedance
HS	Horizontal Synchronization
H/W	Hardware
I/O	Input/Output pin
IC	Integrated Circuit
IBIS	Input/Output Buffer Information Specification
IDD	Analog power supply current
IDDI	Digital power supply current
I/F	Interface
Idle	8-colour mode
ISO	International Organization for Standardization
LC	Liquid Crystal
LCD	Liquid Crystal Display
LSB	Least Significant Bit
LUT	Look Up table
MCU	Micro Controller Unit
MSB	Most Significant Bit
N/A	Not Applicable
PCLK	Pixel Clock
ppi	pixels per inch
pps	points per second
PT	Product Technologies
PWB(PCB)	Printed Wiring Board (Printed Circuit Board) PWM
	Pulse Width Modulation
RAM	Random Access Memory
RDX	Read function in 8080 MCU I/F, the display start to control data bus lines when there is a falling edge of the RDX and the host reads data bus lines when there is a rising edge of the RDX
RESX	Reset H/W Control pin, active Low
RGB	Red, Green, Blue
RH	Relative Humidity
RT	Room Temperature
S/W	Software
SoC	Statement of Conformance

Ta	Ambient Temperature
TBD	To Be Defined
TP	Technology Platforms
TR	Transflective LC type
TRC	Tone Rendering Curve (Gamma)
TM	Transmissive LC type
VCC	Digital power supply voltage (for Driver internal digital power supply)
VCOMAC	Command Amplitude voltage
VCOMH	Command High level voltage
VCOML	Command Low level voltage
VCI1	Booster input voltage (regulator from VDD)
VCL	VCOML supply voltage
VDD	Analog (Booster) power supply voltage
VDDI	Logic (I/O) power supply voltage
VS	Vertical Synchronization
VSS	System Ground
WRX	Write function in 8080 MCU I/F, the host start to control data bus lines when there is a falling edge of the WRX and the display reads data bus lines when there is a rising edge of the WRX

INDEX

REVISION HISTORY

Date	Contents	Version
Oct. 14, 2005	- Preliminary Version 0.0	Ver. 0.0.0
Oct. 31 2005	-Add pin SCL and REGP(Page 11,13) -Modify pin description -Modify RGB i/f bus width set (Page 52) -Modify MCU and RGB Interface comparison (Page 68) -Modify reset table -Add VSYNC I/F (Page 98) -Add VSYNC and gamma separator register setting item	Ver. 0.0.1
Nov. 11 2005	-Modify MCU and RGB Interface comparison (Page 73) -Modify VSYNC I/F -Add SPI_CSX pin(Page 13)	Ver. 0.0.2
Nov. 14 2005	-Add display resolution -Modify chip version code (Page 168) -Modify Booster circuit Step-up cycle RC2h~RC4h (Page 186,188,190)	Ver. 0.0.3
Nov. 22 2005	-Modify some item relative to display resolution.	Ver. 0.0.4
JAN.6 2006	- Add SPI RGB read GRAM format -18-Bits Parallel Interface Set Table -Modify the booster circuit step-up cycle -Modify gamma structure -Modify test pin (Page 18) -Add pin assignment and coordinate	Ver. 0.0.5
JAN.13 2006	-Modify R09h description -Modify RC5h description	Ver. 0.0.6
JUNE.15 2006	-Gamma structure _Serial Interface Characteristics -Add 4-wire serial interface select -Modify MTP Access Sequence for Program	Ver. 0.0.7
JULY. 5 2006	-Modify 18-Bits Parallel Interface	Ver. 0.0.8
July 21 2006	- Modify MTP Access Sequence for Program	Ver. 1.0.0
Nov 17 2006	- Modify 8080-series MCU 8,9,16,18 BUS tCSH value (Page 241)	Ver. 1.0.1

1 DESCRIPTION

The NT3916 is one chip solution for TFT-LCD panel: source driver with built-in memory, gate driver, power IC are integrated on one chip. This IC can display to a maximum of 176-RGB x 220 -dot graphics on 262k-color TFT panel.

The NT3916 supports 18-/16-/9-/8-bit high-speed bus interface and serial peripheral interfaces (SPI). It also supplies 18-bit, 16-bit or 6-bit RGB interface for driving Video signal directly from controller. The moving picture area can be specified in internal GRAM by window function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

The NT3916 has various functions for reducing the power consumption of a LCD system: operating at low voltage (minimum 1.6V), register-controlled power-save mode, partial display mode and so on. The IC has internal GRAM to store 176-RGB x 220-dot 262k-color image and internal booster that generates the LCD driving voltage, breeder resistance and the voltage follower circuit for LCD driver.

This LSI is suitable for any medium-sized or small portable mobile solution requiring long-term driving capabilities, such as digital cellular phones supporting a web browser, bi-directional pagers, and small PDA.

2. FEATURE

- Chip size: 18.65mm * 1.05mm (include of scribe line)
- Single chip AM-TFT-LCD Controller/ driver with Display RAM.
- Display resolution: 176RGB (H) *220(V)
- Display data RAM (frame memory): 176 x 220 x 18-bits = 696960 bits
- Operation Frequency: ~10MHz
- Output:
  - 528ch source outputs (176RGB)
  - 220ch Gate outputs
  - Common electrode output
- Display mode (Color mode)
  - Full color mode (Idle mode off): 262K-colors
  - Reduce color mode (Idle mode on): 8-colors (3-bits binary mode)
- Display resolution option
  - 176 x 220 Display with 176 x 18-bits x 220 display RAM
  - 176 x 176 Display with 176 x 18-bits x 176 display RAM
  - 176 x 132 Display with 176 x 18-bits x 132 display RAM
- Different LC type option
  - TM LC type (When LCM = “01”)
  - ECB LC type (When LCM = “11”)
- Interface mode (Color modes on the display host interface):
  - 12-bits/Pixel: RGB= (444) using the 696k-bits frame memory and LUT.
  - 16-bits/Pixel: RGB= (565) using the 696k-bits frame memory and LUT.
  - 18-bits/Pixel: RGB= (666) using the 696k-bits frame memory and LUT.
- MCU Interface:
  - 3-pin 9 bits serial interface
  - 8-bits, 9-bits, 16-bits, 18-bits interface with 8080-series MCU
  - 8-bits, 9-bits, 16-bits, 18-bits interface with 6800-series MCU
  - 6-bits, 16-bits, 18-bits RGB interface with graphic controller
- Separate R,G,B gamma control function
- Display features
  - Area scrolling
  - Partial display mode
  - Software programmable color depth mode
- On chip

- DC/DC converter
- Adjusted VCOM generation
- NV Memory to store initialization register setting
- Oscillator for display clock generation
- Timing generation
- 14 preset gamma curve selectable
- Factory default value (Contrast, Module ID, Module version, etc) are stored on the display module
- Line inversion, frame inversion

◆ NV Memory
- 7-bits for ID2
- 8-bits for ID3
- 7-bits for VCOM adjustment

◆ Supply voltage range
- Analog supply voltage range for VDD to AGND: 2.6V – 3.5V
- I/O supply voltage range for VDDI to DGND: 1.6V –3.5V
- Internal Digital supply voltage range for VCC to DGND: **1.5V – 2.0V**

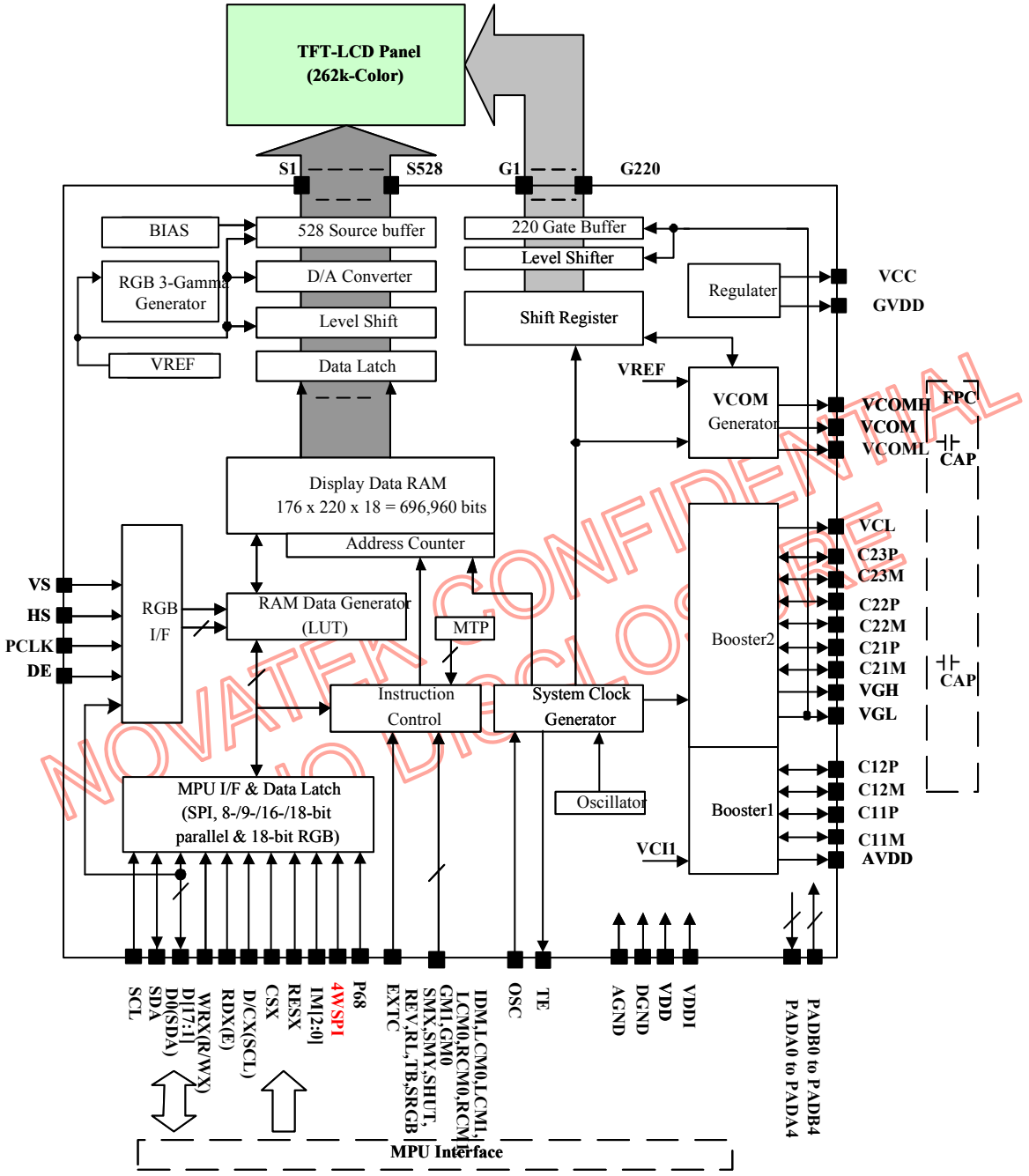
◆ Output voltage levels
- Source output voltage range for GVDD to AGND: 3.0V to 5.0V
- Power supply for driver circuit range for AVDD to AGND: 4.75V to 5.5V
- Common electrode output High voltage range for VCOMH to AGND: 2.5V to 5.0V
- Common electrode output Low voltage range for VCOML to AGND: -2.5V to 0.0V
- Positive Gate output voltage range for VGH to AGND: +10.0V to +13.5V
- Negative Gate output voltage range for VGL to AGND: –11.5V to –9.0V

◆ Lower power consumption, suitable for battery operated systems
- CMOS compatible inputs
- Optimized layout for COG assembly
- Operate Temperature range: -40℃ to +85℃

Note 1: Blank display means: Normal White display = White display, Normal Black display = Black display

Note 2. The display interface does not support any noise recovery, external temperature or light sensing circuit. It needs a copy and detailed explanation of the implementation.

3 BLOCK DIAGRAM



4. DRIVER IC PIN DESCRIPTION

The Abbreviation and vocabulary of pins need be fix at the further.

4.1 Power Supply Pins

Table 4.1.1: Power Supply Pins

Symbol	Name	Description
VDD	Analog voltage	Power supply for analog system and booster system
VDDI	Logic voltage	Power supply for I/O system
AGND	Analog GND	System ground for Analog and Booster system
DGND	Logic GND	System Ground for I/O system and internal digital system

4.2 Interface Logic pins

Table 4.2.1: Interface Logic Pins

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>P68</td><td>I</td><td>-8080 /6800 MCU Interface mode select
<table><tr><th>P68</th><th>Interface mode select</th></tr><tr><td>0</td><td>8080-MCU parallel interface</td></tr><tr><td>1</td><td>6800-MCU parallel interface</td></tr></table>-If not used, please fix this pin at VDDI or DGND level.</td></tr>
<tr><td>IM2, IM1, IM0</td><td>I</td><td>-MCU Parallel interface bus and Serial interface select
<table><tr><th>IM2</th><th>MCU & SPI Interface mode select</th></tr><tr><td>0</td><td>SPI interface</td></tr><tr><td>1</td><td>MCU parallel interface</td></tr></table>-If not used, please fix this pin at VDDI or DGND level.</td></tr>
<tr><td>4WSPI</td><td></td><td>3-pins and 4-pins serial interface select
<table><tr><th>4WSPI</th><th>SPI Interface mode select</th></tr><tr><td>0</td><td>3-pins serial interface select</td></tr><tr><td>1</td><td>4-pins serial interface select</td></tr></table>-If not used, please fix this pin at DGND level.</td></tr>
<tr><td>RESX</td><td>I</td><td>-This signal low. will reset the device and must be applied to properly initialize the chip.
-Signal is active L.</td></tr>
<tr><td>CSX</td><td>I</td><td>-Chip select input pin (“Low” enable).
<table><tr><th>RCM1,RCM0</th><th>IM2</th><th>Data bus format select</th></tr><tr><td>“0X”</td><td>X</td><td>Chip select input pin (“Low” enable)</td></tr><tr><th>RCM1,RCM0</th><th>ICM</th><th>Data bus format select</th></tr><tr><td rowspan="2">“1X”</td><td>0</td><td>Chip select input pin (“Low” enable)</td></tr><tr><td>1</td><td>Chip select input pin (“Low” enable)</td></tr></table>-This pin can be permanently fixed “Low” in MCU & SPI interface mode only.</td></tr>
<tr><td>D/CX (SCL)</td><td>I</td><td>-Display data / Command selection pin in parallel interface.
<table><tr><th>RCM1,RCM0</th><th>IM2</th><th>D/CX</th><th>D/CX format select</th></tr><tr><td rowspan="3">“00”</td><td>0</td><td>-</td><td>This Pin is SPI data clock (SCL)</td></tr><tr><td rowspan="2">1</td><td>0</td><td>Command Register from data bus</td></tr><tr><td>1</td><td>Command parameter or Display data from data bus</td></tr><tr><td rowspan="3"></td><td>0</td><td>-</td><td>CSX should be ignored (In SPI Interface)</td></tr><tr><td rowspan="2">X</td><td>0</td><td>Command Register from data bus</td></tr><tr><td>1</td><td>Command parameter or Display data from data bus</td></tr><tr><td>“1X”</td><td>X</td><td>-</td><td>Not use</td></tr></table>-If not used, please fix this pin at VDDI or DGND level.</td></tr>
</table>

<table>
<tr><td>RDX (E)</td><td>I</td><td>-(RDX) Read enable in 8080-parallel interface.
<table><tr><th>P68</th><th>IM2</th><th>RDX(E) format select</th></tr><tr><td>X</td><td>0</td><td>RDX(E) should be ignored</td></tr><tr><td>0</td><td rowspan="2">1</td><td>(RXD) Read enable in 8080-parallel interface.</td></tr><tr><td>1</td><td>(E) Read/ Write operation enable pin in 6800-parallel interface.</td></tr></table>-(E) Read/ Write operation enable pin in 6800-parallel interface.
<table><tr><th>R/WX</th><th>E</th><th>RDX(E) format select</th></tr><tr><td>0</td><td>↓</td><td>Write operation enable pin in 6800-parallel interface.</td></tr><tr><td>1</td><td>↓</td><td>Read operation enable pin in 6800-parallel interface.</td></tr></table>-If not used, please connect to ground or VDDI this pin</td></tr>
<tr><td>WRX (R/WX)
(SPI_DCX)</td><td>I</td><td>-(WRX) Write enable in parallel interface
-(R/WX) Read/Write select pin in 6800-Parallel interface
<table><tr><th>P68</th><th>4WSPI</th><th>IM2</th><th>RDX(E) format select</th></tr><tr><td>X</td><td>0</td><td>0</td><td>WRX(R/WX) should be ignored</td></tr><tr><td>X</td><td>1</td><td>0</td><td>SPI_DCX is used as Serial input/ output signal</td></tr><tr><td>0</td><td rowspan="2">X</td><td rowspan="2">1</td><td>(WRX) Write enable in 8080-parallel interface.</td></tr><tr><td>1</td><td>(R/WX) Read/Write operation enable pin in 6800-parallel interface.</td></tr></table>-If not used, please connect to ground or VDDI this pin</td></tr>
<tr><td>D[17:0]
D0(SDA)</td><td>I/O</td><td>-Data bus
<table><tr><th>RCM1,RCM0</th><th>IM2</th><th>Data bus format select</th></tr><tr><td rowspan="2">“00”</td><td>0</td><td>1. D[17:1] should be ignored (In SPI Interface)
2. D0 is used as Serial input/ output signal</td></tr><tr><td>1</td><td>D[17:0] are used for MCU interface data bus</td></tr><tr><td rowspan="2">“01”</td><td>0</td><td>D[17:0] should be ignored (In SPI Interface)</td></tr><tr><td>1</td><td>D[17:0] are used for MCU interface data bus</td></tr><tr><th>RCM1,RCM0</th><th>ICM</th><th>Data bus format select</th></tr><tr><td rowspan="2">“1X”</td><td>0</td><td>D[17:0] are used for RGB interface data bus</td></tr><tr><td>1</td><td>D[17:0] should be ignored (In SPI Interface)</td></tr></table></td></tr>
<tr><td>TE</td><td>O</td><td>-Tearing effect output pin to synchronies MCU to frame writing, activated by S/W command.
-When this pin is not activated (TE function off), this pin is low.
<table><tr><th>S/W</th><th>ECTC function format</th></tr><tr><td>34h</td><td>DGND level (TE off)</td></tr><tr><td>35h</td><td>To synchronies MCU to frame writing</td></tr></table>-If not used, please open this pin.</td></tr>
<tr><td>SPI_CSX</td><td>I</td><td>-It is used as Serial interface chip select signal (“Low” enable).</td></tr>
<tr><td>SCL</td><td>I</td><td>-It is used as Serial clock signal.
<table><tr><th>RCM1,RCM0</th><th>IM2</th><th>SCL format select</th></tr><tr><td>“00”</td><td>‘x’</td><td>Not use</td></tr><tr><td rowspan="2">“01”</td><td>0</td><td>Serial clock signal in SPI I/F mode.</td></tr><tr><td>1</td><td>SCL should be ignored (In MCU Interface)</td></tr><tr><th>RCM1,RCM0</th><th>ICM</th><th>SCL format select</th></tr><tr><td>“1X”</td><td>‘x’</td><td>Serial clock signal in SPI I/F mode.</td></tr></table>-If not used, please connect to ground or VDDI this pin interface</td></tr>
<tr><td>SDA</td><td>I/O</td><td>-It is used as Serial input/ output signal.</td></tr>
</table>

<table>
<tr><td></td><td></td><td>
<table>
<tr><th>RCM1,RCM0</th><th>IM2</th><th>SDAL format select</th></tr>
<tr><td>“00”</td><td>‘x’</td><td>Not use</td></tr>
<tr><td rowspan="2">“01”</td><td>0</td><td>Serial input/ output signal in serial I/F mode.</td></tr>
<tr><td>1</td><td>SDA should be ignored (In MCU Interface)</td></tr>
<tr><th>RCM1,RCM0</th><th>ICM</th><th>SDA format select</th></tr>
<tr><td>“1X”</td><td>‘x’</td><td>Serial input/output signal in serial I/F mode.</td></tr>
</table>
-In SPI I/F
-This data is input on the rising edge of the SCL signal
-This data is output on the falling edge of the SCL signal
-If not used, please fix this pin at VDDI or DGND level.
</td></tr>
<tr><td>PCLK</td><td>I</td><td>
-Pixel clock signal in RGB I/F mode.
<table>
<tr><th>RCM1,RCM0</th><th>--</th><th>HS signal mode select</th></tr>
<tr><td>“0x”</td><td>‘x’</td><td>Not use</td></tr>
<tr><th>RCM1,RCM0</th><th>ICM</th><th>HS signal mode select</th></tr>
<tr><td rowspan="2">“1x”</td><td>0</td><td>Pixel clock signal in RBG I/F mode</td></tr>
<tr><td>1</td><td>This pin should be ignored (In SPI Interface)</td></tr>
</table>
-If not used, please fix this pin at VDDI or DGND level.
</td></tr>
<tr><td>VS</td><td>I</td><td>
-Vertical sync. Signal in RGB I/F &VSYNC I/F mode.
<table>
<tr><th>RCM1,RCM0</th><th colspan="2">VS signal mode select</th></tr>
<tr><td colspan="2">“00”</td><td>This pin no use,fix this pin at VDDI or DGND level</td></tr>
<tr><td colspan="2">“01”</td><td>Vertical sync. Signal in VSYNC I/F</td></tr>
<tr><th>RCM1,RCM0</th><th>ICM</th><th>VS signal mode select</th></tr>
<tr><td rowspan="2">“1X”</td><td>0</td><td>Vertical sync.signal in RBG I/F</td></tr>
<tr><td>1</td><td>This pin should be ignored (SPI I/F)</td></tr>
</table>
-If not used, please fix this pin at VDDI or DGND level.
</td></tr>
<tr><td>HS</td><td>I</td><td>
-Horizontal sync. Signal in RGB I/F mode.
<table>
<tr><th>RCM1,RCM0</th><th>--</th><th>HS signal mode select</th></tr>
<tr><td>“0x”</td><td>‘X’</td><td>Not use</td></tr>
<tr><th>RCM1,RCM0</th><th>ICM</th><th>HS signal mode select</th></tr>
<tr><td rowspan="2">“1X”</td><td>0</td><td>Horizontal sync.signal in RBG I/F</td></tr>
<tr><td>1</td><td>This pin should be ignored (SPI I/F)</td></tr>
</table>
-If not used, please fix this pin at VDDI or DGND level.
</td></tr>
<tr><td>DE</td><td>I</td><td>
-Data enable signal in RGB I/F mode.
<table>
<tr><th>RCM1,RCM0</th><th>--</th><th>HS signal mode select</th></tr>
<tr><td>“0x”</td><td>‘X’</td><td>Not use</td></tr>
<tr><th>RCM1,RCM0</th><th>ICM</th><th>HS signal mode select</th></tr>
<tr><td rowspan="2">“1X”</td><td>0</td><td>Data enable signal in RBG I/F</td></tr>
<tr><td>1</td><td>This pin should be ignored (SPI I/F)</td></tr>
</table>
-If not used, please fix this pin at VDDI or DGND level.
</td></tr>
</table>

Note1. If CSX is connected to ground in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Furthermore there will be no influence to the Power Consumption of the display module.

Note2. When in 8 line parallel mode (IM1, IM0=”0””) then id some data or signal appears on D[15:8] then it will have no influence to the system. (D[15:8] can be connected to 1 or 0)

Note3. When CSX= 1 , there is no influence to the parallel and serial interface.

Note4. 1 = VDDI level, 0 = DGND level.

4.3 Mode Selection pins

Table 4.3.1: Mode Selection Pins

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>EXTC</td><td>I</td><td>-To use extended command set (like EEPROM program), please connect this pin to VDDI. During normal operation, please open this pin. (internal Rpull-down=15KΩ)
-EXCT='1', use extended command table (command value can be modify by external command table)
-EXCT='0', only use default command value
-If not used, please fix this pin at VDDI or DGND level.</td></tr>
<tr><td>GM1, GM0</td><td>I</td><td>-Panel resolution selection pins.
<table>
<tr><th>GM</th><th>Resolution selection</th></tr>
<tr><td>00</td><td>176RGB x 220(S1~S528 and G1~G220 output)</td></tr>
<tr><td>01</td><td>176RGB x 176(S1~S528 and G1~G176 output)</td></tr>
<tr><td>10</td><td>Reserved</td></tr>
<tr><td>11</td><td>176RGB x 132(S1~S528 and G1~G132 output)</td></tr>
</table></td></tr>
<tr><td>LCM1, LCM0</td><td>I</td><td>-Different Liquid Crystal (LC) type selection pins.
<table>
<tr><th colspan="2">LCM1, LCM0</th><th>LC type selection</th></tr>
<tr><td>00</td><td>0</td><td>Reserved</td></tr>
<tr><td>01</td><td>1</td><td>TM (Transmission) LC type</td></tr>
<tr><td>10</td><td>2</td><td>Reserved</td></tr>
<tr><td>11</td><td>3</td><td>ECB LC Type (Separate RGB Gamma)</td></tr>
</table>
-If not used, please fix this pin at VDDI or DGND level.</td></tr>
<tr><td>RCM1, RCM0</td><td>I</td><td>- RGB and MCU interface mode selection pin.
<table>
<tr><th colspan="2">RCM1,RCM0</th><th>Resolution selection</th></tr>
<tr><td>00</td><td>0</td><td>MCU interface mode (1)</td></tr>
<tr><td>01</td><td>1</td><td>MCU interface mode (2)</td></tr>
<tr><td>10</td><td>2</td><td>RGB Interface (1)</td></tr>
<tr><td>11</td><td>3</td><td>RGB Interface (2)</td></tr>
</table>
-If not used, please fix this pin at VDDI or DGND level.</td></tr>
<tr><td>SRGB</td><td>I</td><td>-RGB direction select H/W pin for Color filter default setting.
<table>
<tr><th>SRGB</th><th>RGB filter order for Color filter default setting</th></tr>
<tr><td>0</td><td>S1, S2, S3 filter order = 'R', 'G', 'B'</td></tr>
<tr><td>1</td><td>S1, S2, S3 filter order = 'B', 'G', 'R'</td></tr>
</table>
-Please refer chapter 10 for detail using
-If not used, please fix this pin at VDDI or DGND level.</td></tr>
<tr><td>SMX</td><td>I</td><td>-Module source output direction H/W select pin
<table>
<tr><th>SMX</th><th>Module source output direction</th></tr>
<tr><td>0</td><td>S1 -> S528</td></tr>
<tr><td>1</td><td>S528 -> S1</td></tr>
</table>
-Please refer chapter 10 for detail using
-If not used, please fix this pin at VDDI or DGND level.</td></tr>
<tr><td>SMY</td><td>I</td><td>-Module Gate output direction H/W select pin
<table>
<tr><th>SMY</th><th colspan="3">Module Gate output direction</th></tr>
<tr><td></td><td>GM=00</td><td>GM=01</td><td>GM=11</td></tr>
<tr><td>0</td><td>G1 -> G220</td><td>G1 -> G176</td><td>G1 -> G132</td></tr>
<tr><td>1</td><td>G220 -> G1</td><td>G176 -> G1</td><td>G132 -> G1</td></tr>
</table>
-Please refer chapter 10 for detail using
-If not used, please fix this pin at VDDI or DGND level.</td></tr>
</table>

IDM — I

-Normal mode and Idle mode control pin

-Please refer RGB I/F for detail using.

IDM	Idle mode H/W controller
0	Normal display (can be changed to Idle mode by S/W)
1	Into Idle mode

-If not used, please fix this pin at VDDI or DGND level.

SHUT — I

-Display On/ Off H/W control pin In RGB I/F

-Please refer RGB I/F for detail using.

SHUT	Display On/Off in RGB I/F
0	Display On
1	Display Off

-If not used, please fix this pin at VDDI or DGND level.

RL — I

-Source output direction H/W select pin in RGB I/F

-Please refer RGB I/F for detail using.

RL	Module source output direction
0	**S1** -> S528
1	S528 -> **S1**

-If not used, please fix this pin at VDDI or DGND level.

TB — I

-Gate output direction H/W select pin on RGB I/F

-Please refer RGB I/F for detail using.

When SMY=0

SMY	Module Gate output direction		
	GM=00	GM=01	GM=11
0	**G1** -> G220	**G1** -> G176	**G1** -> G132
1	G220 -> **G1**	G176 -> **G1**	G132 -> **G1**

When SMY=1

SMY	Module Gate output direction		
	GM=00	GM=01	GM=11
0	G220 -> **G1**	G176 -> **G1**	G132 -> **G1**
1	**G1** -> G220	**G1** -> G176	**G1** -> G132

-If not used, please fix this pin at VDDI or DGND level.

REV — I

-Source output data polarity select H/W pin.

-Please refer RGB I/F for detail using.

REV	Source output data polarity in RGB I/F
0	Data not reverse
1	Data reverse

-If not used, please fix this pin at VDDI or DGND level.

4.4 Driver Output Pins

Table 4.4.1: Driver output Pins

Symbol	I/O	Description
S1 to S528	O	-Source driver output pins.
G1 to G220	O	-Gate driver output pins.
VCI1	I/O	-A reference voltage in step-up circuit 1. -Connect a capacitor for stabilization.
AVDD	O	-A power output pin for source driver block that is generated from power block -Output of booster 1 circuit (output of 2-times output of VCI1 or VDD) -Connect a capacitor for stabilization.
VCL	O	-A power supply pin for generating VCOML. -Connect a capacitor for stabilization.
VGH	O	-Positive voltage of the Booster circuit 2 -Connect a capacitor for stabilization.
VGL	O	-Negative voltage of the Booster circuit 3 -Connect a capacitor for stabilization.
VREF	O	-Reference voltage for power block. -Connect a capacitor for stabilization.
GVDD	O	-A standard level for grayscale voltage generator -Connect a capacitor for stabilization.
VCOMH	O	-Positive voltage output of VCOM -Connect a capacitor for stabilization.
VCOML	O	-Negative voltage output of VCOM -Connect a capacitor for stabilization.
VCOM	O	-A power supply for the TFT common electrode.
C11P, C11N C12P, C12N	O	-Capacitor connecting pins for Booster circuit 1 (for AVDD)
C21P, C21N C22P, C22N C23P, C24N	O	-Capacitor connecting pins for Booster circuit 2 (for VGH, VGL, VCL)
VDDIO	O	-VDDI voltage output level for control pins using
DGNDO	O	-DGND voltage output level for control pins using
VCC	O	-Power supply for internal digital system

4.5 Miscellaneous Control Pins

Table 4.5.1: Miscellaneous Control Pins

Symbol	I/O	Description
PREG	I	-Select VCC power when sleep in mode -REGP=0:When VDDI<2.0V -REGP=1:When VDDI>2.0V

4.6 Test Pins

Table 4.6.1: Driver output Pins

Symbol	I/O	Description
PADA0	O	-These test pins for display glass break detection. -If not used, please open these pins.
PADB0	I	
PADA1	O	-These test pins for chip attachment detection. -If not used, please open these pins.
PADB1	I	
PADA2	O	
PADB2	I	
PADA3	O	
PADB3	I	
PADA4	O	
PADB4	I	
Test[1]~[20]	I/O	-These test pins for Driver vender test used. -If not used, please open these pins.
DUMMYA[A]~[23] DUMMYB[1] DUMMC[1],[2]		-These pins are dummy (not have any function inside) -Can have signal traces pass through on TFT glass under the PAD.

5 FUNCTIONAL DESCRIPTION

5.1 MPU Interface

5.1.1 Interface Type Selection

The selection of a given interfaces are done by setting P68, IM2, IM1, and IM0 pins as show in Table 5.1.1 and Table 5.1.2.

Table 5.1.1 MCU Interface Type Selection

P68	4WSPI	IM2	IM1	IM0	Interface	Read back selection
-	0	0	-	-	3-Pin Serial interface	Via the read instruction (12-bit, 16-bit and 18-bit read parameter
-	1	0	-	-	4-Pin Serial interface	Via the read instruction (12-bit, 16-bit and 18-bit read parameter
0	-	1	0	0	8080 MCU 8-bit Parallel	RDX strobe (8-bit read data and 8-bit read parameter)
0	-	1	0	1	8080 MCU 16-bit Parallel	RDX strobe (16-bit read data and 8-bit read parameter)
0	-	1	1	0	8080 MCU 9-bit Parallel	RDX strobe (9-bit read data and 8-bit read parameter)
0	-	1	1	1	8080 MCU 18-bit Parallel	RDX strobe (18-bit read data and 8-bit read parameter)
1	-	1	0	0	6800 MCU 8-bit Parallel	E strobe (8-bit read data and 8-bit read parameter)
1	-	1	0	1	6800 MCU 16-bit Parallel	E strobe (9-bit read data and 8-bit read parameter)
1	-	1	1	0	6800 MCU 9-bit Parallel	E strobe (16-bit read data and 8-bit read parameter)
1	-	1	1	1	6800 MCU 18-bit Parallel	E strobe (18-bit read data and 8-bit read parameter)

Table 5.1.2 Pin connection According to MCU Interface Type Selection

P68	4WSPI	IM2	IM1	IM0	Interface	RDX	WRX	D/CX	Read back selection
-	0	0	-	-	3-Pin Serial interface	Note1	Note 1	SCL	D[17:1]: Unused, D0: SDA
-	1	0	-	-	4-Pin Serial interface	Note1	Note 1	SCL	D[17:1]: Unused, D0:SDA,WRX:SPI_DCX
0	-	1	0	0	8080 MCU 8-bit Parallel	RDX	WRX	D/CX	D[17:8]: Unused, D7-D0: 8-bit Data
0	-	1	0	1	8080 MCU 16-bit Parallel	RDX	WRX	D/CX	D[17:16]: Unused, D15-D0: 16-bit Data
0	-	1	1	0	8080 MCU 9-bit Parallel	RDX	WRX	D/CX	D[17:9]: Unused, D8-D0: 9-bit Data
0	-	1	1	1	8080 MCU 18-bit Parallel	RDX	WRX	D/CX	D17-D0: 18-bit Data
1	-	1	0	0	6800 MCU 8-bit Parallel	E	WRX	RS	D[17:8]: Unused,D7-D0:8-bit Data
1	-	1	0	1	6800 MCU 16-bit Parallel	E	WRX	RS	D[17:16]: Unused, D15-D0: 16-bit Data
1	-	1	1	0	6800 MCU 9-bit Parallel	E	WRX	RS	D[17:9]: Unused,D8-D0:9-bit Data
1	-	1	1	1	6800 MCU 18-bit Parallel	E	WRX	RS	D17-D0: 18-bit Data

Note 1. Unused pins can be open, connected to DGND or VDDI level.

5.1.2 8080-Series Parallel Interface (P68='0')

The MCU uses a 11-wires 8-data parallel interface or 12-wires 9-data parallel interface or 19-wires 16-data parallel interface or 21-wires 18-data parallel interface. The chip-select CSX(active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write, RDX is the parallel data read and D[17:0] is parallel data.
The Graphics Controller Chip reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits are display RAM data or command parameters. When D/C='0', D[17:0] bits are commands.
The 6800-series bi-directional interface can be used for communication between the micro controller and LCD driver chip. The selection of this interface is done when P68 pin is low state (DGND). Interface bus width can be selected with IM2, IM1 and IM0.
The interface function of 8080-series parallel interface are given in Table5.1.2.1

Table 5.1.2.1 The function of 8080-series parallel interface

P68	IM2	IM1	IM0	Interface	D/CX	RDX	WRX	Function
0	1	0	0	8-bit Parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 8-bit display data or 8-bit parameter (D7 to D0)
					1	↑	1	Read 8-bit Display data (D7 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)
0	1	0	1	16-bit Parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 16-bit display data or 8-bit parameter (D15 to D0)
					1	↑	1	Read 16-bit Display data (D15 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)
0	1	1	0	9-bit Parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 9-bit display data or 8-bit parameter (D8 to D0)
					1	↑	1	Read 9-bit Display data (D8 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)
0	1	1	1	18-bit Parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 18-bit display data or 8-bit parameter (D17 to D0)
					1	↑	1	Read 18-bit Display data (D17 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)

Note: applied for command code: DAh, DBh, DCh, 04h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh.

Write cycle sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control (D/CX, RDX, WRX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data (='1')

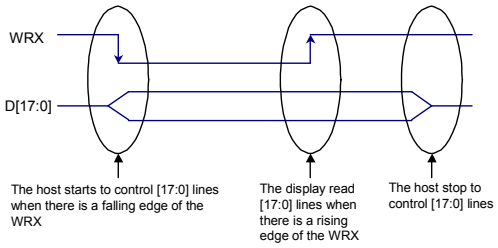


Fig.5.1.2.1 8080-series WRX Protocol

Note: WRX is an unsynchronized signal (It can be stopped)

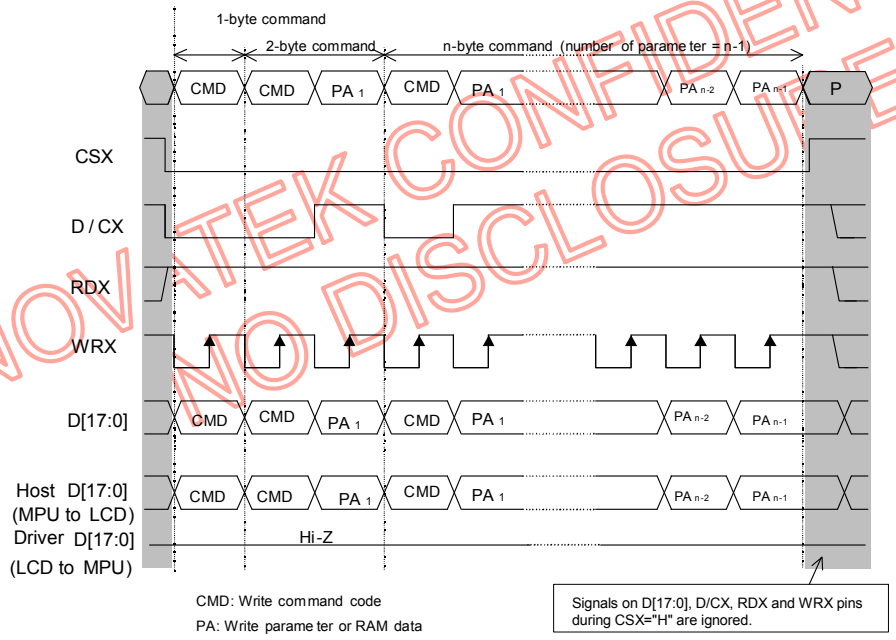


Fig.5.1.2.2 8080-Series Parallel bus Protocol (Write to register or display RAM)

Read Cycle Sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from display via interface. The display sends data (D[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

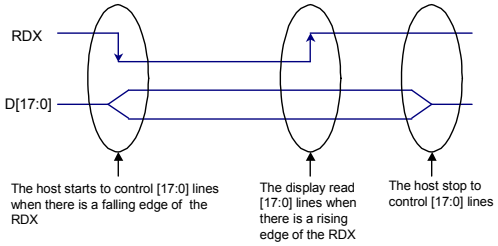


Fig.5.1.2.1 8080-series RDX Protocol

Note: RDX is an unsynchronized signal (It can be stopped)

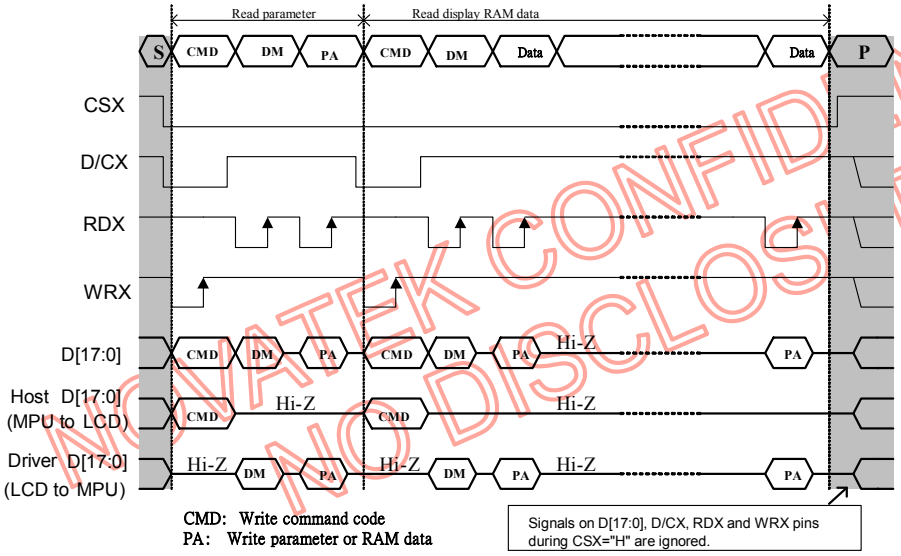


Fig. 5.1.2.4 8080-Series Parallel bus protocol (Read from register or display RAM)

5.1.3 6800-Series Parallel Interface (P68='1')

The MCU uses a 11-wires 8-data parallel interface or 12-wires 9-data parallel interface or 19-wires 16-data parallel interface or 21-wires 18-data parallel interface. The chip-select CSX(active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. The R/WX is the Read/Write flag and D[17:0] is parallel data.
The Graphics Controller Chip reads the data at the falling edge of E signal when R/WX= '1' and Writes the data at the falling of the E signal when R/WX='0'. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits are display RAM data or command parameters. When D/C= '0', D[17:0] bits are commands.
The 6800-series bi-directional interface can be used for communication between the micro controller and LCD driver chip. The selection of this interface is done when P68 pin is high state (VDDI). Interface bus width can be selected with IM2, IM1 and IM0.
The interface functions of 6800-series parallel interface are given in Table 5.1.3

Table 5.1.3 The function of 6800-series parallel interface

P68	IM2	IM1	IM0	Interface	D/CX	R/WX	E	Function
1	1	0	0	8-bit interface	0	0	↓	Write 8-bit command (D7 to D0)
					1	0	↓	Write 8-bit display data or 8-bit parameter (D7 to D0)
					1	1	↓	Read 8-bit display data (D7 to D0)
					1	1	↓	Read 8-bit parameter or status (D7 to D0)
1	1	0	1	16-bit interface	0	0	↓	Write 8-bit command (D7 to D0)
					1	0	↓	Write 16-bit display data or 8-bit parameter (D15 to D0)
					1	1	↓	Read 16-bit display data (D15 to D0)
					1	1	↓	Read 8-bit parameter or status (D7 to D0)
1	1	1	0	9-bit interface	0	0	↓	Write 8-bit command (D7 to D0)
					1	0	↓	Write 9-bit display data or 8-bit parameter (D8 to D0)
					1	1	↓	Read 9-bit display data (D8 to D0)
					1	1	↓	Read 8-bit parameter or status (D7 to D0)
1	1	1	1	18-bit interface	0	0	↓	Write 8-bit command (D17 to D0)
					1	0	↓	Write 18-bit display data or 8-bit parameter (D17 to D0)
					1	1	↓	Read 18-bit display data (D7 to D0)
					1	1	↓	Read 8-bit parameter or status (D7 to D0)

Note: applied for command code: DAh, DBh, DCh, 04h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh.

Write cycle sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (E low-high-low sequence) consists of 3 control (D/CX, E, R/WX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (=’0’) and vice versa it is data (=’1’).

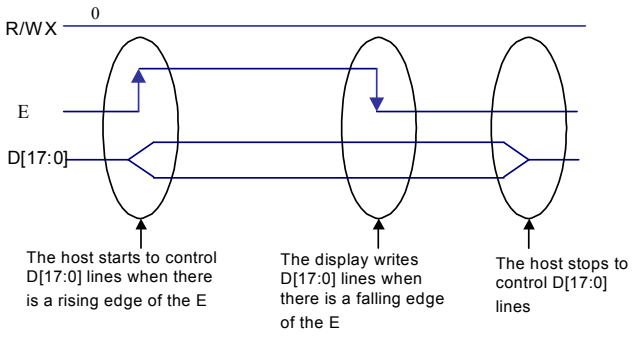


Fig. 5.1.3.1 6800-Series Write Protocol

Note: E is an unsynchronized signal (It can be stopped)

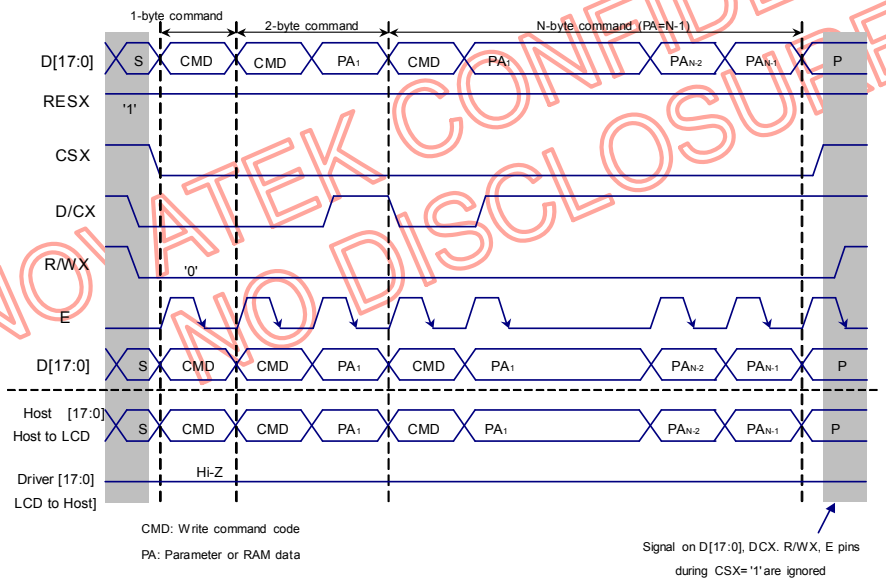


Fig. 5.1.3.2 6800-Series parallel bus protocol, Write to register or display RAM

Read Cycle Sequence

The write cycle means that the host reads information (command or/and data) to the display via the interface. Each read cycle (E low-high-low sequence) consists of 3 control (D/CX, E, R/WX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (=’0’) and vice versa it is data (=’1’).

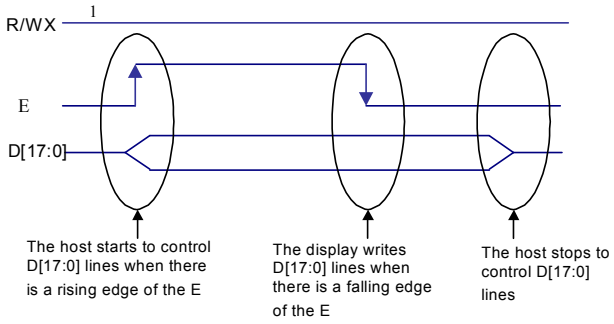


Fig. 5.1.3.3 6800-Series Read Protocol

Note: E is an unsynchronized signal (It can be stopped)

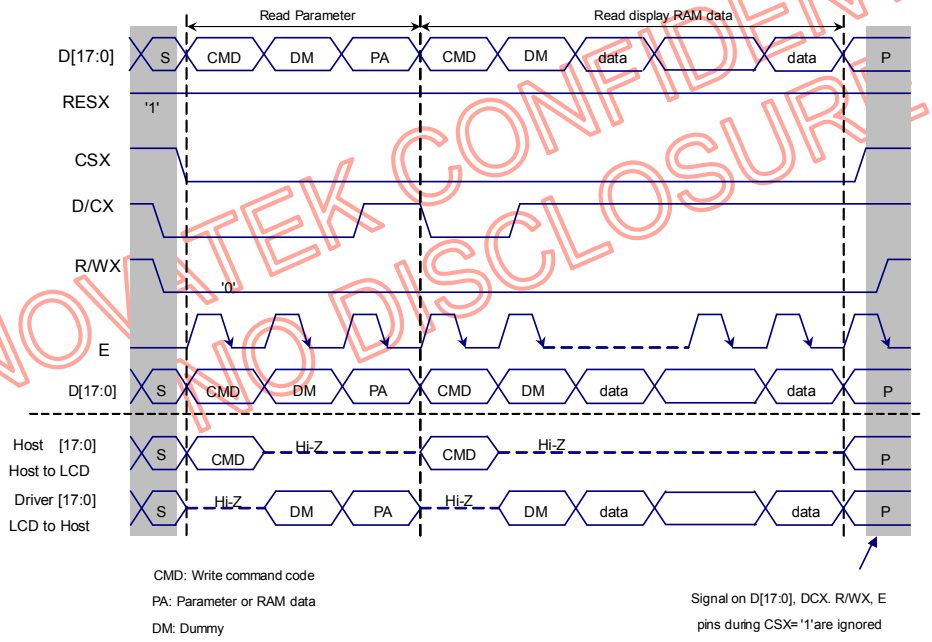


Fig. 5.1.3.4 6800-Series parallel bus protocol, Read data from register or display RAM

5.1.4 Serial Interface

The selection of this interface is done by P68, IM2, IM1 and IM0. See the Table 8.4.1. Table 8.4.1 Serial Interface Type Selection

P68	4WSPI	IM2	IM1	IM0	Interface	Read back selection
--	0	0	--	--	3-Pin Serial interface	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)
--	1	0	--	--	4-Pin Serial interface	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)

The serial interface is a 3-pin 9-bit or 4-pin-8-bit bi-directional interface for communication between the micro controller and the LCD driver chip. The 3-pin serial use: CSX (chip enable), SCL(serial clock) and SDA (serial data input/output)and the 4-pins serial use:CSX (chip enable),D/CX (data/command select),SCL (serial clock)and SDA (serial data input/output). Serial clock(SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

Command Write Mode

The write mode of the interface means the micro controller writes commands and data to the 3-Pin serial data packet contains a control bit D/CX and a transmission byte. If D/CX is low, the transmission byte is interpreted as command byteand in 4-pins serial case, data packet contains just transmission byte and control bit D/CX is transfrerred by the D/CX pin . If D/CX is high, the transmission byte is stored in the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to the DRIVER. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

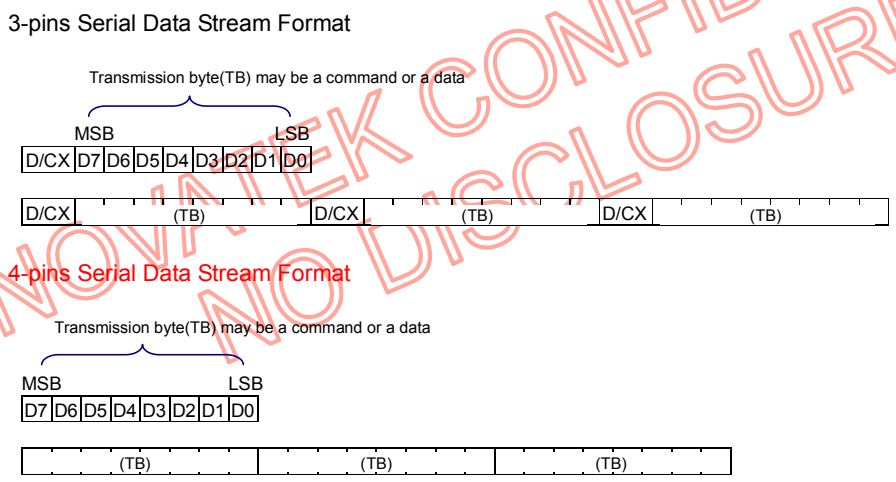


Fig. 5.1.4.1 Serial interface data Stream format

When CSX is high, SCL clock is ignored. During the high time of CSX the serial interface is initialized. At the falling edge of CSX, SCL can be high or low(see ***Fig 5.1.4.2***). SDA is sampled at the rising edge of CSX. D/CX indicates, whether the byte is command code (D/CX= '0') or parameter/RAM data (D/CX='1'). It is sampled when first rising edge of CSX (3-pin serial interface) or 8th rising edge of SCL (4-pins serial interface). If CSX stay low after the last bit of command/data byte, the serial interface expects the D/CX bit (3-pin serial interface) or D7 (4-pins serial interface) of the next byte at the next rising edge of SCL.

3-pins Serial Interface Protocol

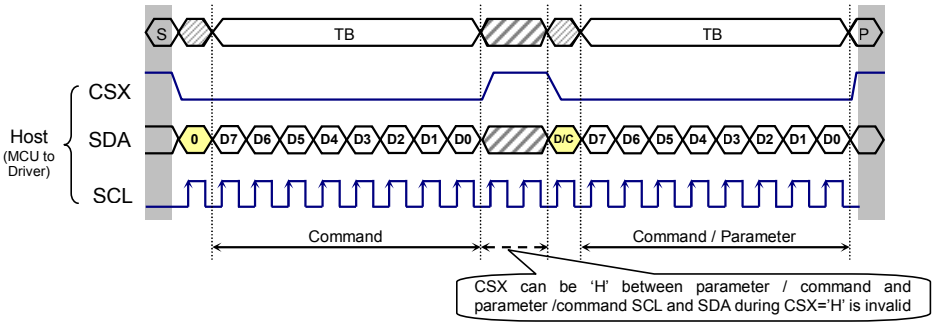


Fig. 5.1.4.2 3-pins Serial interface Write protocol (Write to register with control bit in transmission)

4-pins Serial Interface Protocol

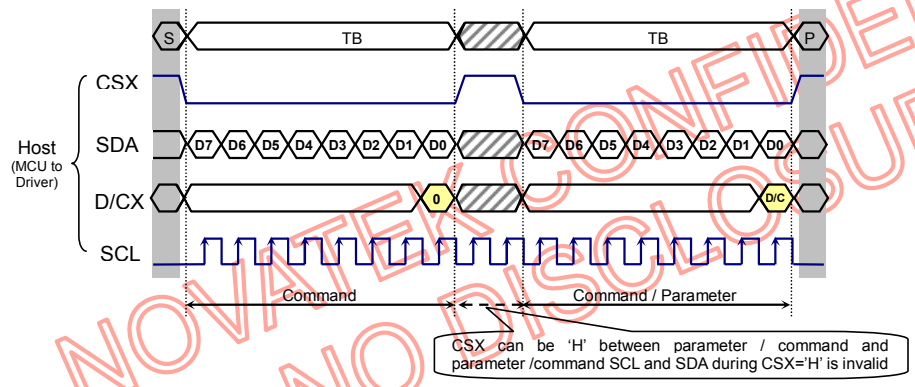
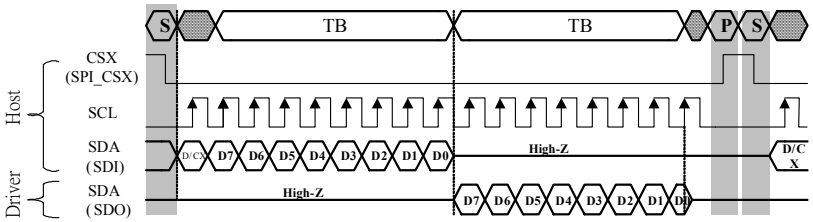


Fig. 5.1.4.3 4-pins Serial interface Write protocol (Write to register with control bit in transmission)

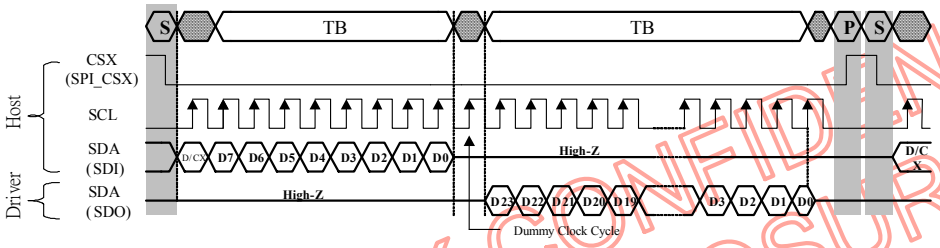
Read Functions

The read mode of the interface means that the micro controller reads register value from the Driver. To do the micro controller first has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

3- Pin Serial Protocol (for RDID1 / RDID2 / RDID3 / 0Ah / 0Bh / 0Ch / 0Dh / 0Eh / 0 Fh command : 8- bit read)



3- Pin Serial Protocol (for RDDID command: 24- bit read)



3- Pin Serial Protocol (for RDDID command: 32- bit read)

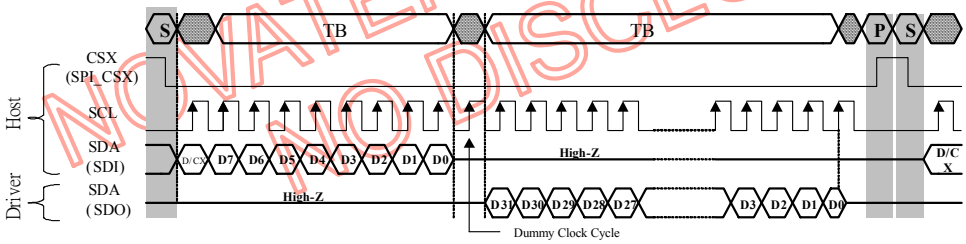
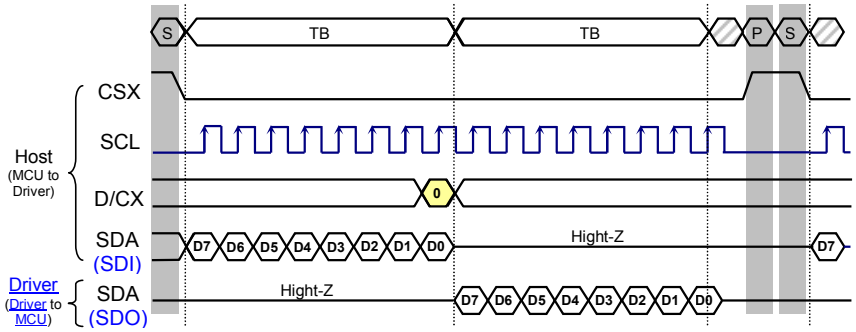
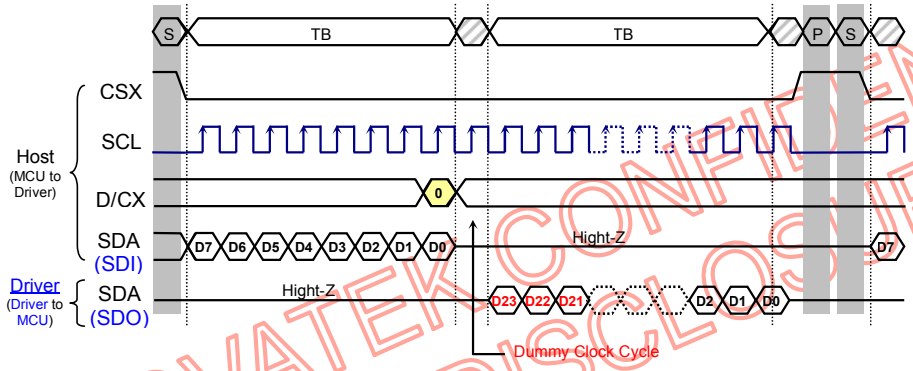


Fig. 5.1.4.3 3-pin Serial interface Read protocol

4-pins Serial Protocol (for RDID1/ RDID2/ RDID3/ 0AH/ 0BH/ 0CH/ 0DH/ 0EH/ 0FH command: 8-bits read)



4-pins Serial Protocol (for RDID command:24-bits read)



4-pins Serial Protocol (for RDST command:32-bits read)

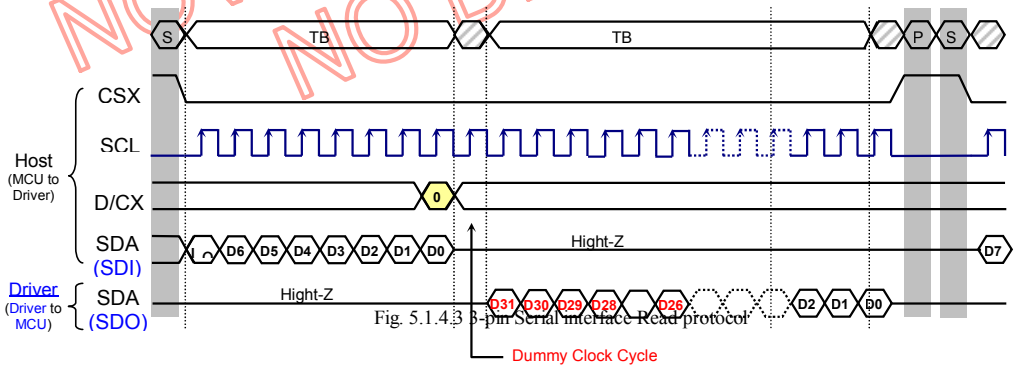


Fig. 5.1.4.3 3-pin Serial Interface Read protocol

5.1.5 Data Transfer Pause

It will be possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then DRIVER will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select Line is released after a whole byte of a command has been completed, then the Display Module will receive either the command 's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below.

This applies to the following 4 conditions:
1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

Serial Interface Pause

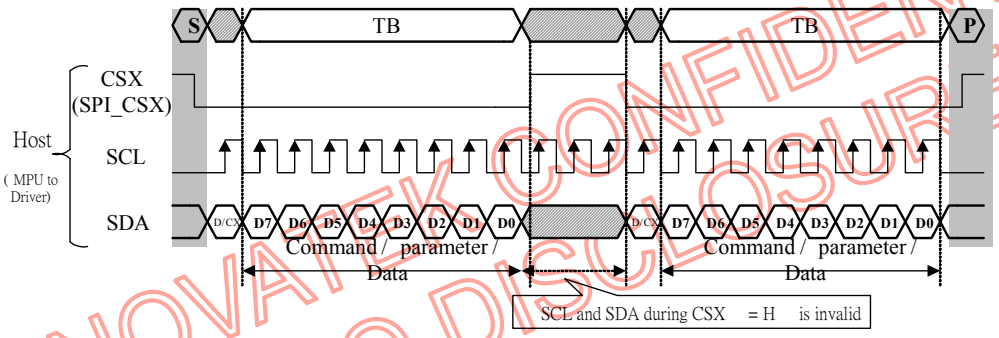


Fig. 5.1.5.1 Serial interface Pause Protocol (pause by CSX)

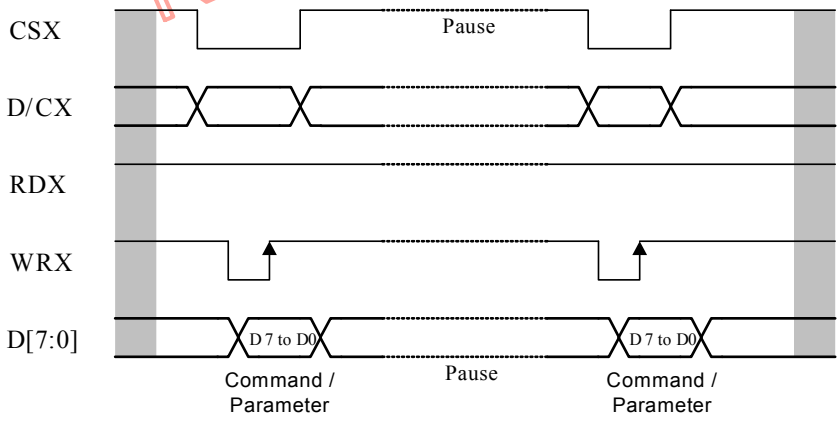


Fig. 5.1.5.2 Parallel bus Pause Protocol (paused by CSX)

5.1.6 Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then DRIVER will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been High state. See the following example

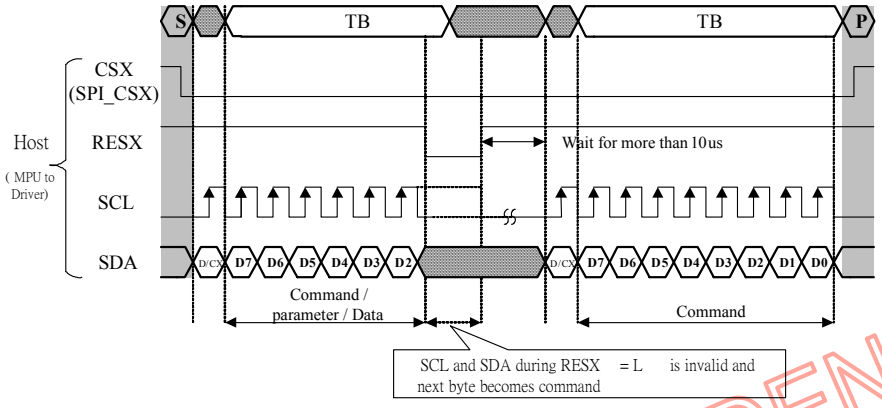
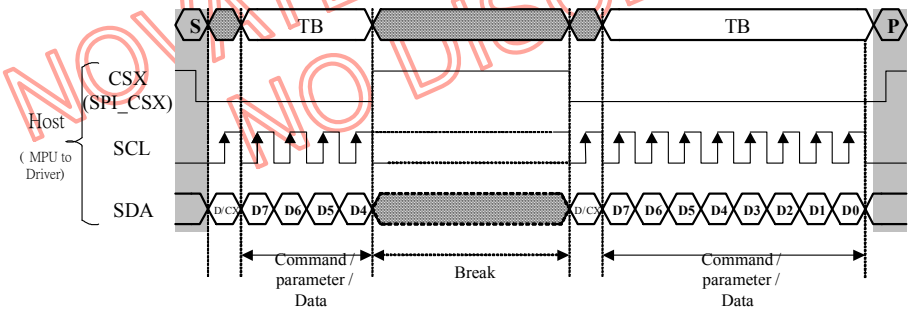


Fig. 5.1.6.1 Serial bus protocol, write mode – interrupted by RESX

If there is a break in data transmission by CSX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then DRIVER will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following example

Fig. 5.1.6.2 Serial bus protocol, write mode – interrupted by CSX



If 1, 2 or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

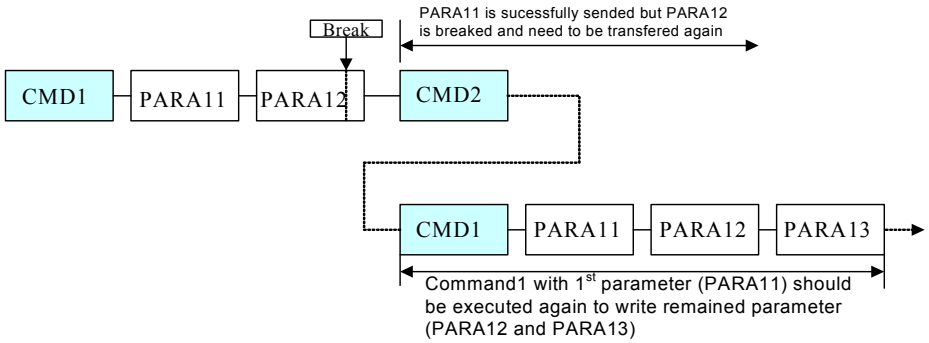


Fig. 5.1.6.3 Write interrupts recovery (serial interface)

If a 2 or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.

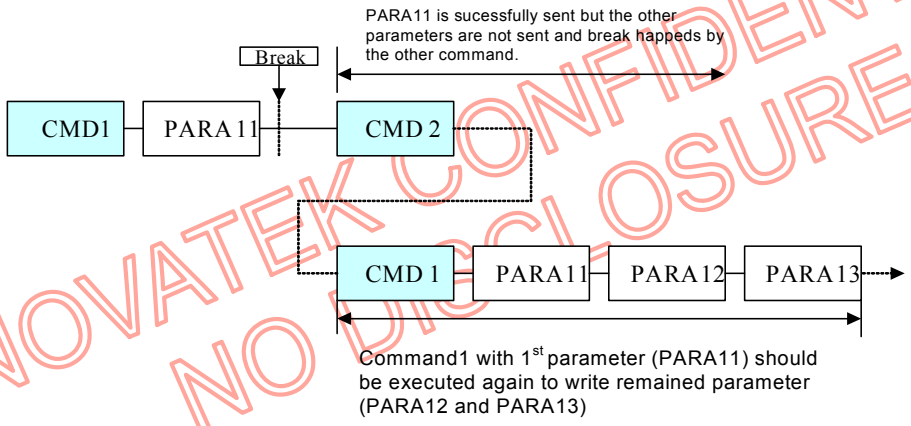


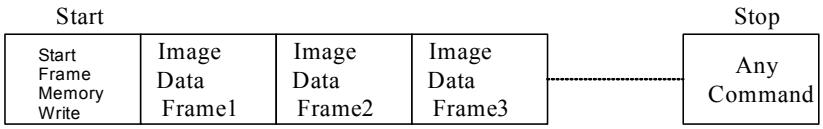
Fig. 5.1.6.4 Write interrupts recovery (both serial and parallel interface)

5.1.7 Display Module Data Transfer Modes

The Module has four kinds colour modes for transferring data to the display RAM. These are 8-bit colour per pixel, 12-bit colour per pixel, 16-bit colour per pixel and 18-bit colour per pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

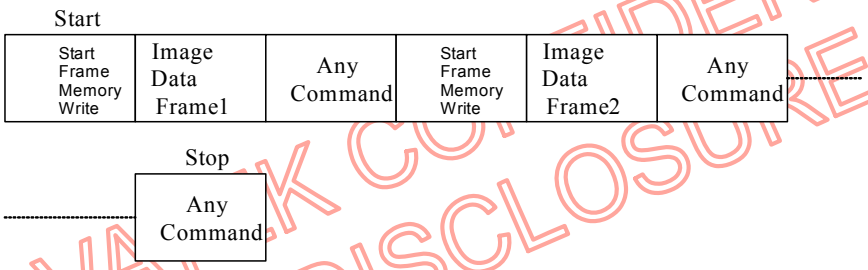
5.1.7.1 Method 1

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written



5.1.7.2 Method 2

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame is downloaded.



Note:

1) These apply to all Data Transfer Color modes on both Serial and Parallel interfaces.

2) The Frame Memory can contain both odd and even number of pixels for both Methods. Only complete pixel data will be stored in the Frame Memory.

5.2 Display Data RAM

The display module has an integrated 176x220x18-bit graphic type static RAM. This 696,960-bits memory allows to store on-chip a 176xRGBx220 image with an 18-bpp resolution (262K-color).

There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

Display Data RAM Organization

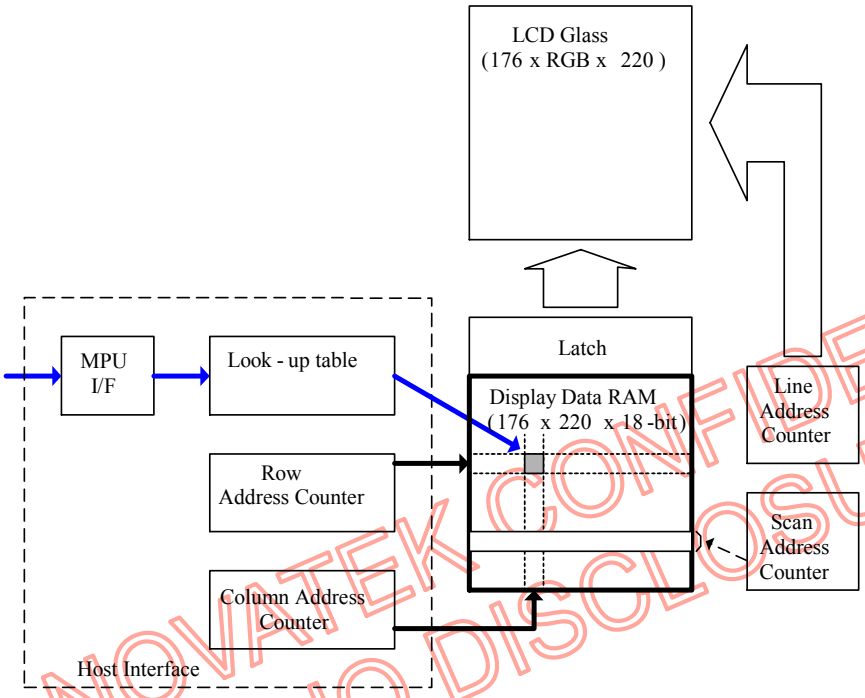


Fig. 5.2 Display Data RAM Organization

5.2.1 Display Data Format

5.2.1.1 8-Bits Parallel Interface (IM2='1', IM1, IM0= "00")

Different display data formats are available for three Colors depth supported by listed below.

- 4k Colors, RGB 4,4,4-bits input, (3Ah="03h")
- 65k Colors, RGB 5,6,5-bits input,(3Ah="05h")
- 262k Colors, RGB 6,6,6-bits input, (3Ah="06h")

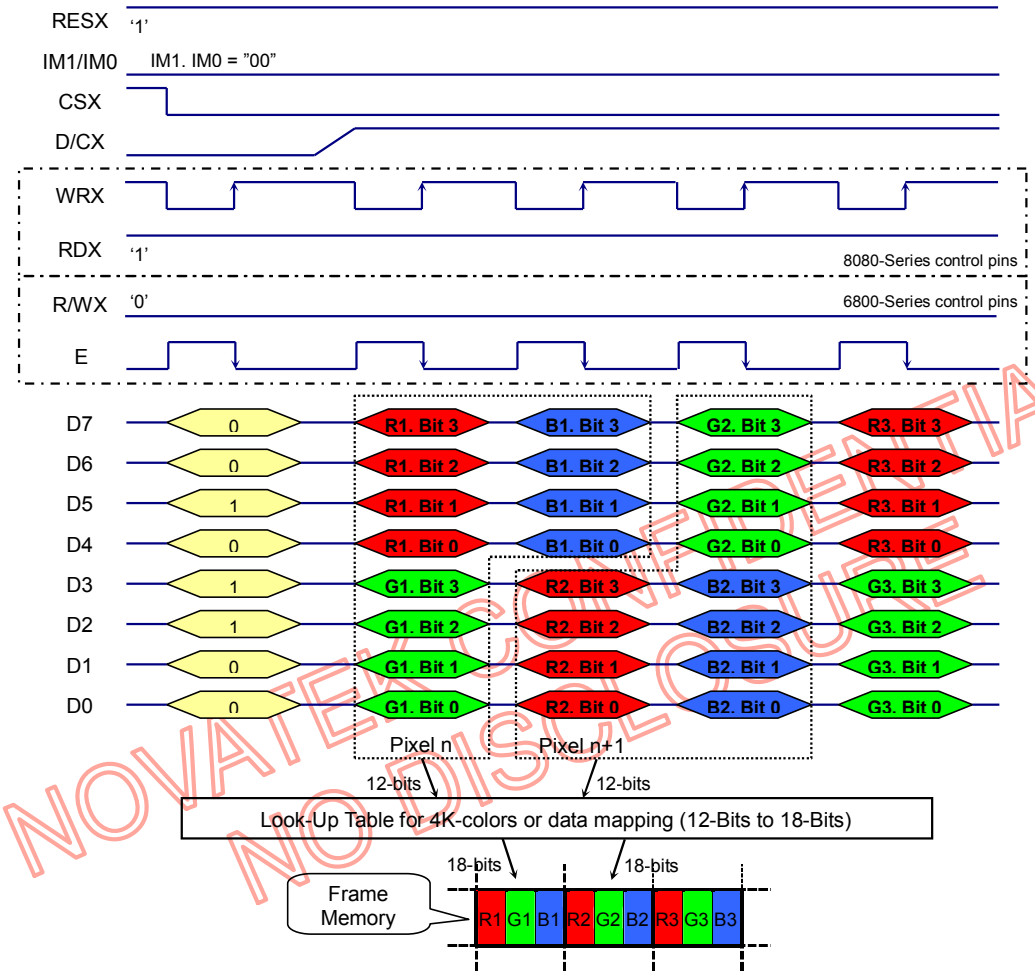
Table 8.8.1.1 8-Bits Parallel Interface Set Table

Register Command		D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
		x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	2Ch
IFPF[2:0]		D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Colour
011	3	x	x	x	x	x	x	x	x	x	x	R3	R2	R1	R0	G3	G2	G1	G0	4K-Colour (2-pixels/ 3-byyes)
		x	x	x	x	x	x	x	x	x	x	B3	B2	B1	B0	R3	R2	R1	R0	
		x	x	x	x	x	x	x	x	x	x	G3	G2	G1	G0	B3	B2	B1	B0	
101	5	x	x	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	65K-Colour (1-pixels/ 2-byyes)
		x	x	x	x	x	x	x	x	x	x	G2	G1	G0	B4	B3	B2	B1	B0	
110	6	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Colour (1-pixels/ 3byyes)
		x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
		x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

3A

Write 8-bit data for RGB 4-4-4-bits input

There are 2 pixels (6 sub-pixels) per 3-transfer. 3AH="03h"



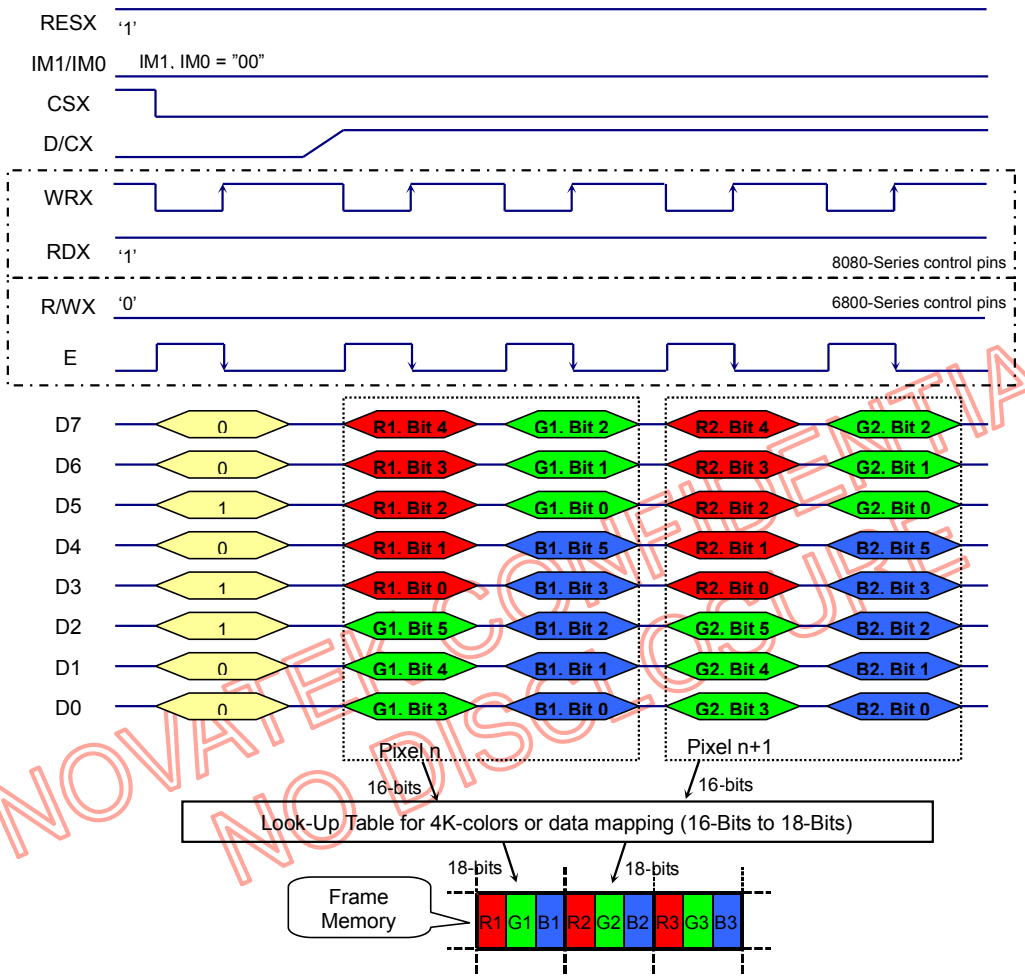
Note1. The data order is ad follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

Note 2.3-times transfer is used to transmit 1 pixel data with the 12-bits color depth information.

Note 3. '-' = Don't care - Can be set to VDDI or DGND level

Write 8-bits data for RGB 5-6-5-bits input

There is 1 pixel (3 sub-pixels) per 2- transfer. 3AH="05h"



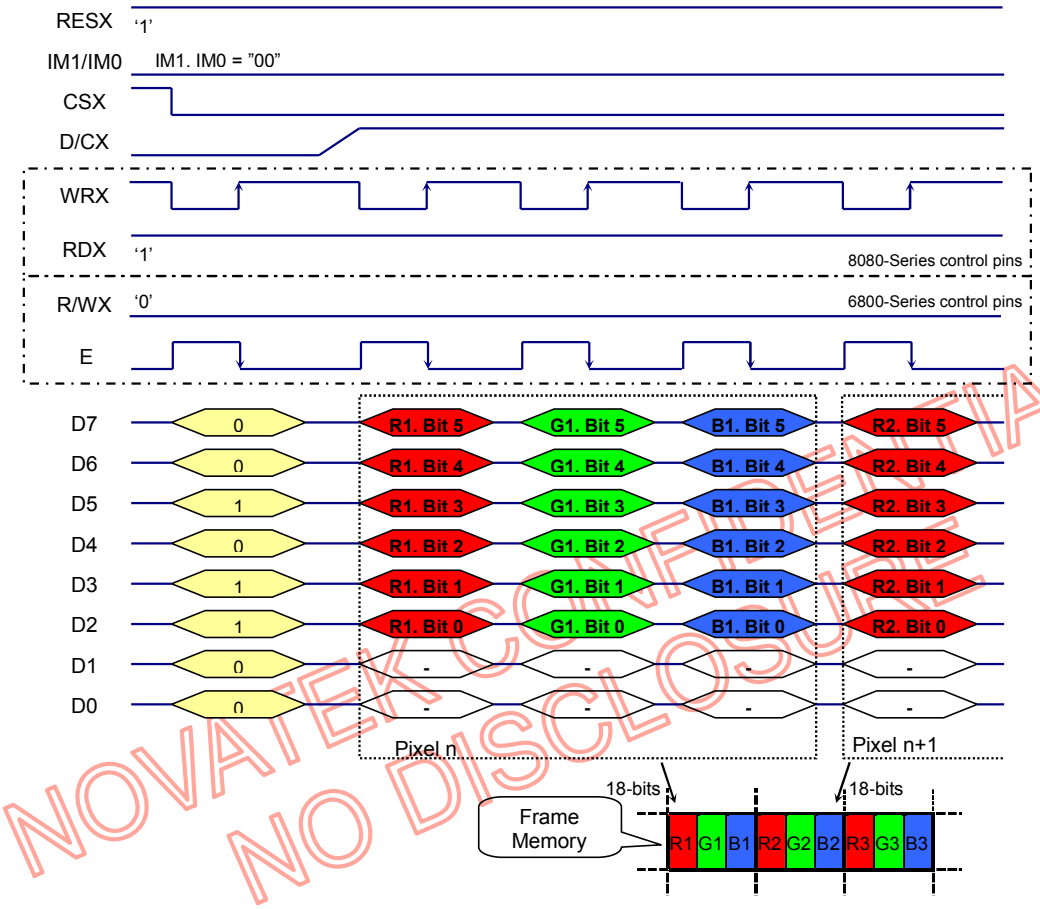
Note1. The data order is ad follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2.2-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.

Note 3. '-' = Don't care - Can be set to VDDI or DGND level

Write 8-bit data for RGB 6-6-6-bits input

There is 1 pixel (3 sub-pixels) per 3- transfer. 3AH="06h"



Note1. The data order is ad follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2.3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Note 3. '-' = Don't care - Can be set to VDDI or DGND level

5.2.1.2 16-Bit Parallel Interface (IM2='1', IM1, IM0="01")

Different display data formats are available for three Colors depth supported by listed below.

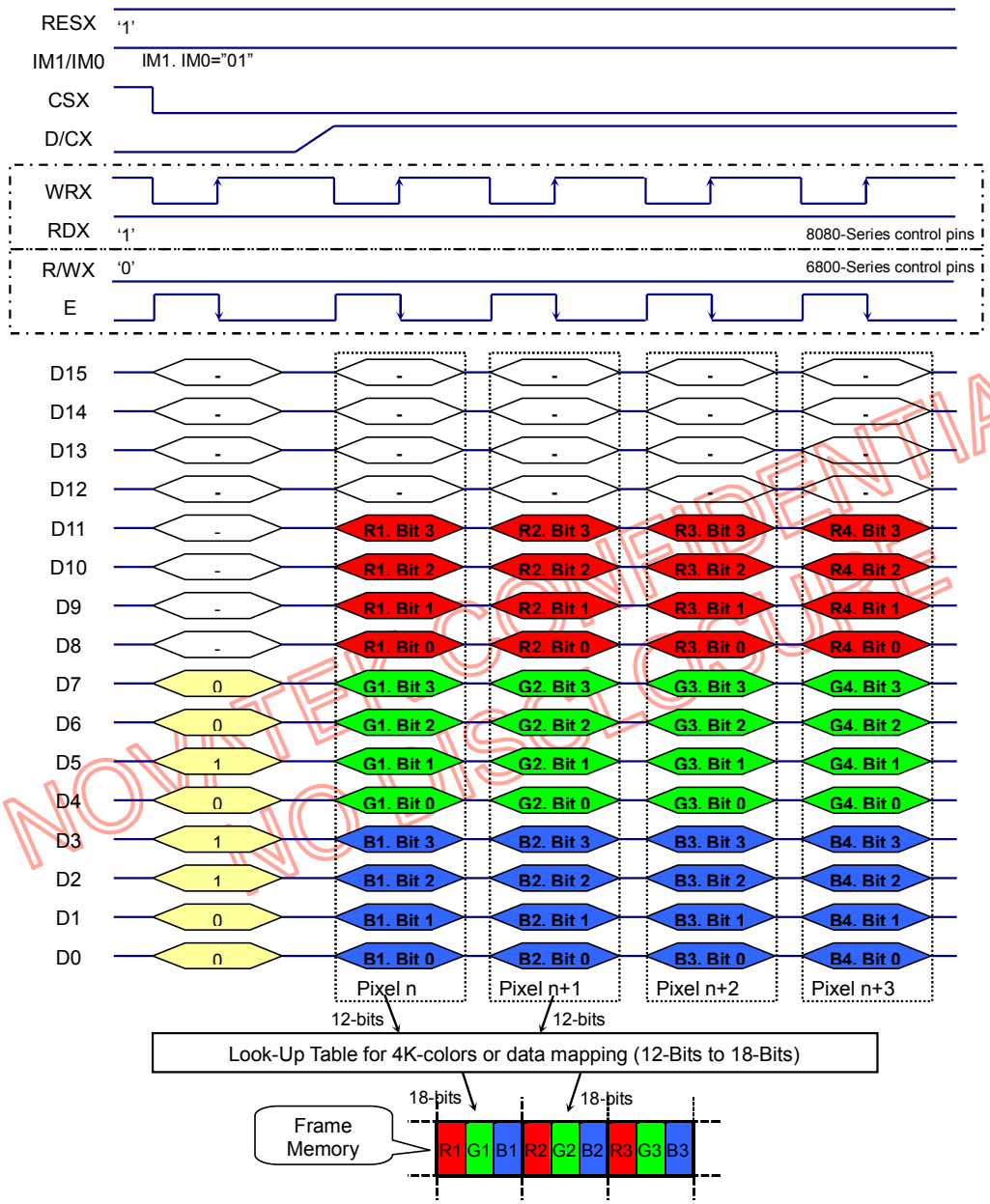
- 4k Colors, RGB 4,4,4-bits input, (3AH="03h")
- 65k Colors, RGB 5,6,5-bits input, (3AH="05h")
- 262k Colors, RGB 6,6,6-bits input, (3AH="06h")

Table 8.8.2.1 16-Bits Parallel Interface Set Table

Register Command		D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
		x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	2Ch
IFPF[2:0]		D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Colour
011	3	x	x	x	x	x	x	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0	4K-Colour
101	5	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	65K-Colour
110	6	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	262K-Colour (2-pixels/ 3byyes)
		x	x	B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x	
		x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x	

Write 16-bit data for RGB 4-4-4-bits input (4k-color)

There is 1 pixel (3 sub-pixels) per 1-transfer, 12-bits/pixel. 3AH="03h"



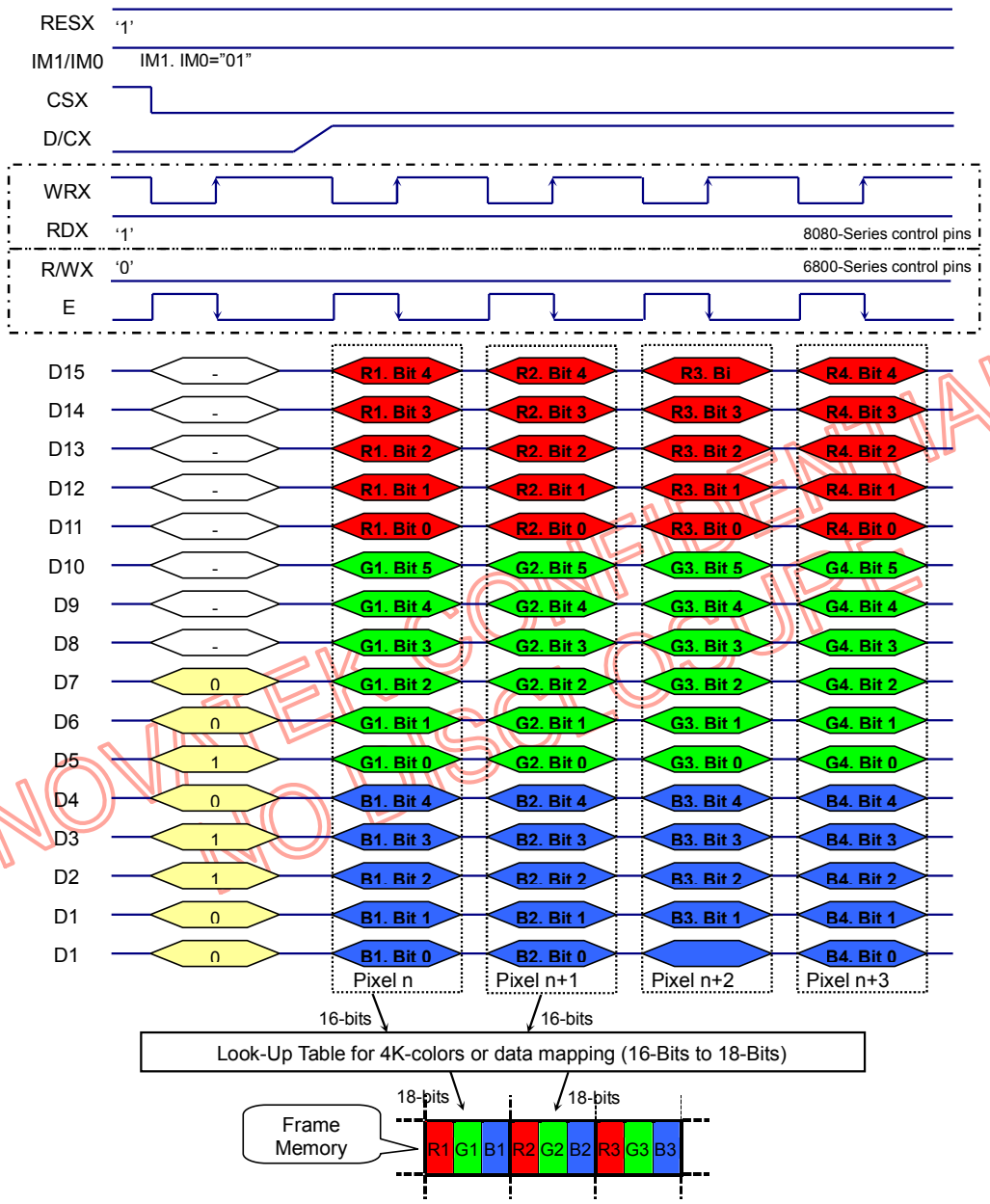
Note1. The data order is ad follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

Note 2.1-times transfer is used to transmit 1 pixel data with the 12-bits color depth information.

Note 3. '-' = Don't care - Can be set to VDDI or DGND level

Write 16-bit data for RGB 5-6-5-bits input (65k-color)

There is 1 pixel (3 sub-pixels) per 1-transfer, 16-bits/pixel. 3AH="05h"



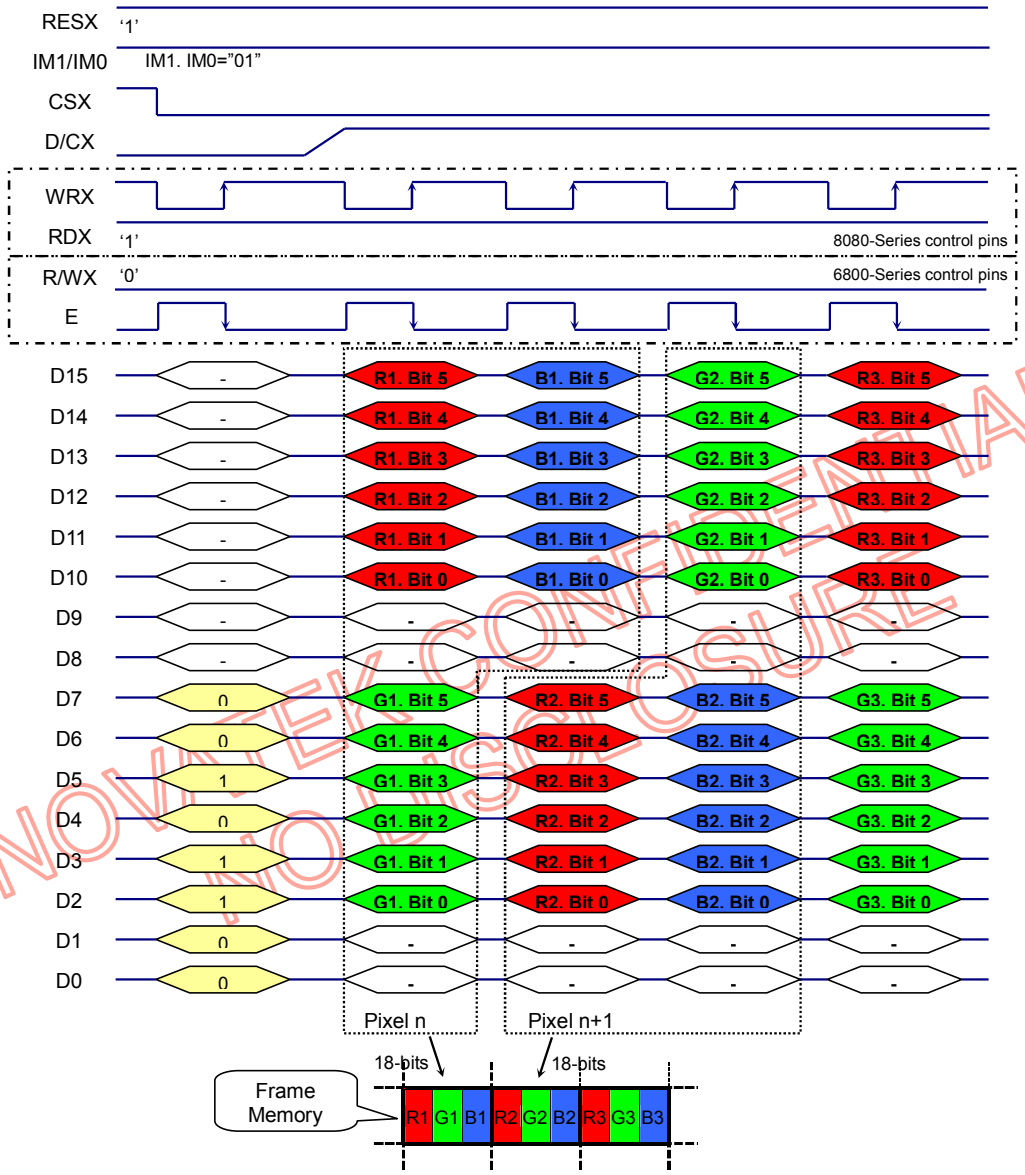
Note1. The data order is ad follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2.1-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.

Note 3. '-' = Don't care - Can be set to VDDI or DGND level

Write 16-bit data for RGB 6-6-6-bits input (262k-color)

There are 2 pixels (6 sub-pixels) per 3-transfer, 18-bit/pixel 3AH="06h"



Note1. The data order is ad follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2.3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Note 3. '-' = Don't care - Can be set to VDDI or DGND level

5.2.1.3 9-Bit Parallel Interface (IM2='1', IM1, IM0="10")

Different display data formats are available for three Colors depth supported by listed below.

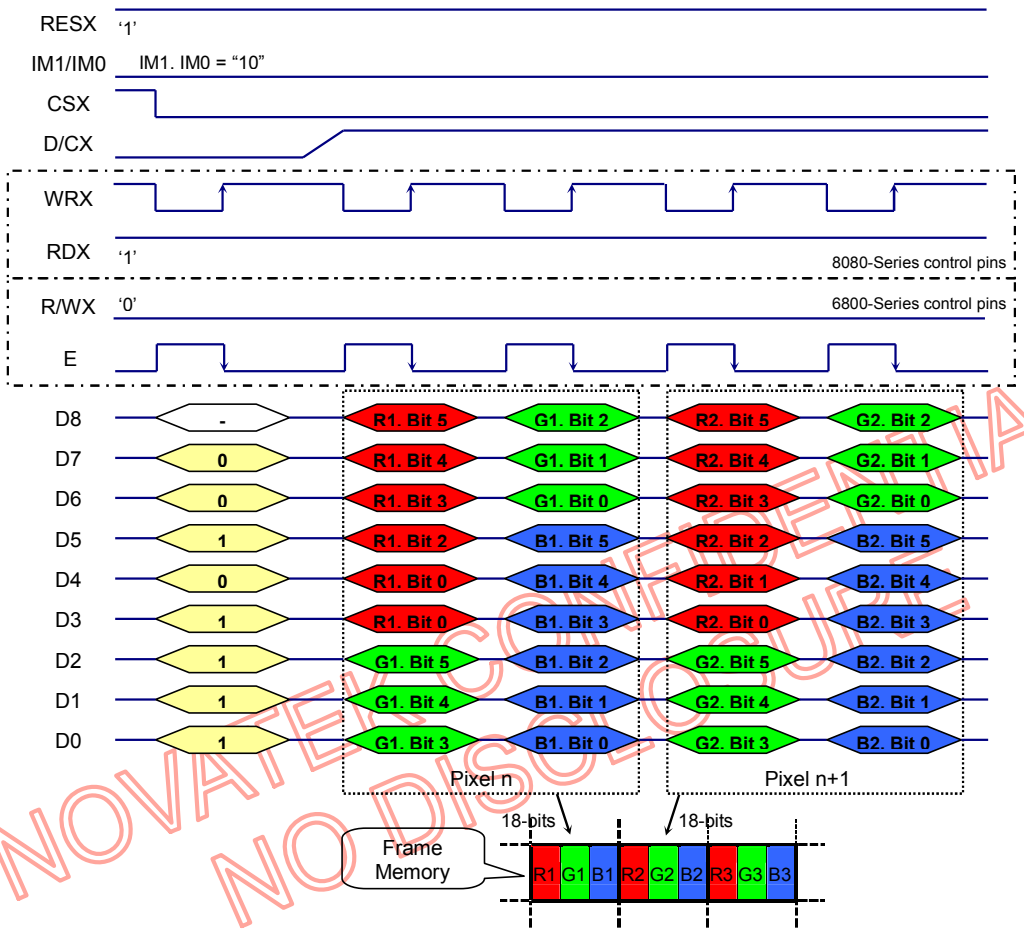
- 262k Colors, RGB 6,6,6-bits input, (3AH="06h")

Table 8.8.3.1 9-Bits Parallel Interface Set Table

Register Command		D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
		x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	2Ch
IFPF[2:0]		D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Colour
110	6	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Colour (1-pixels/ 2byyes)
		x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

Write 9-bit data for RGB 6-6-6-bits input (262k-color)_

There are 2 pixels (6 sub-pixels) per 4-transfer, 18-bits/pixel. 3AH="06h"



Note1. The data order is ad follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2.3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3. '-' = Don't care - Can be set to '0' or '1'

5.2.1.4 18-Bit Parallel Interface (IM2='1', IM1, IM0="11")

Different display data formats are available for three Colors depth supported by listed below.

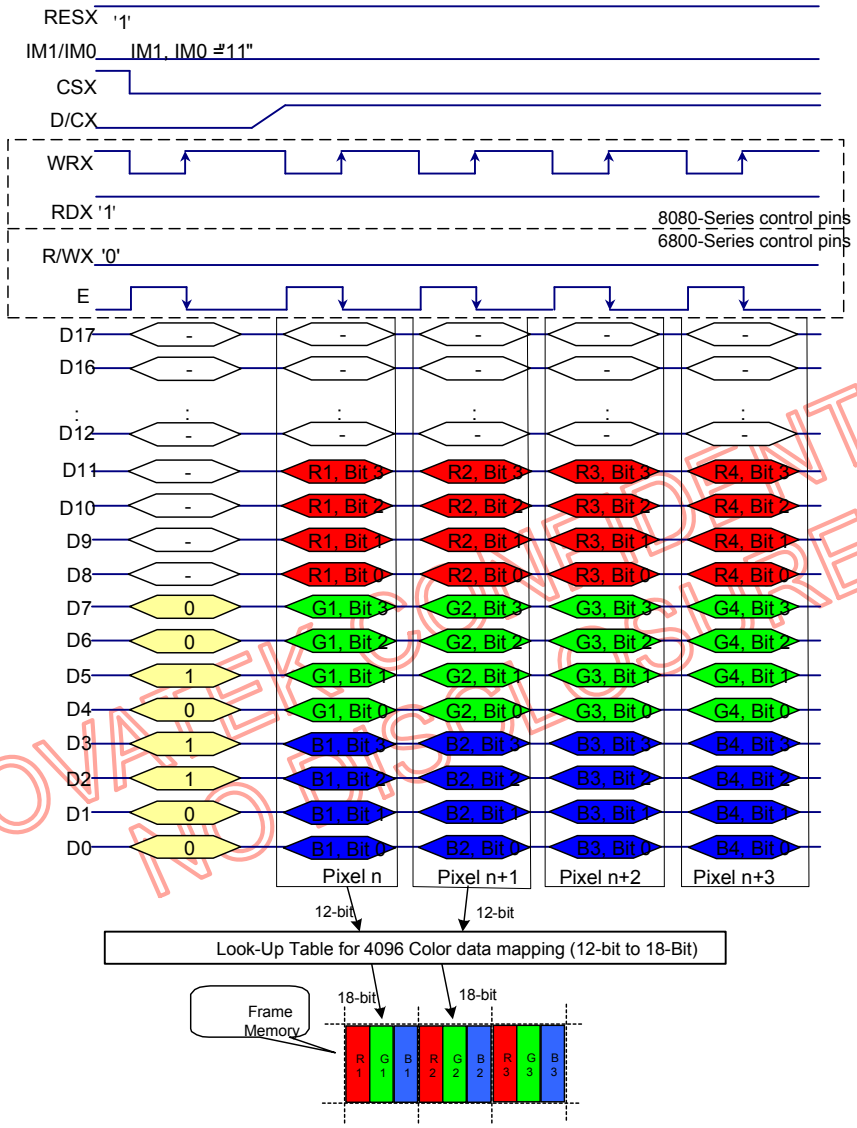
- 4k Colors, RGB 4,4,4-bits input, (3AH="03h")
- 65k Colors, RGB 5,6,5-bits input,(3AH="05h")
- 262k Colors, RGB 6,6,6-bits input, (3AH="06h")

Table 8.8.4.1 18-Bits Parallel Interface Set Table

Register Command		D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
		x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	2Ch
IFPF[2:0]		D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Colour
011	3	x	x	x	x	x	x	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0	4K-Colour
101	5	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	65K-Colour
110	6	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Colour

Write 18-bits data for RGB 4-4-4-bits input (4k-color)

There is 1 pixel (3 sub-pixels) per 1-transfer, 12-bits/pixel. 3AH="03h"

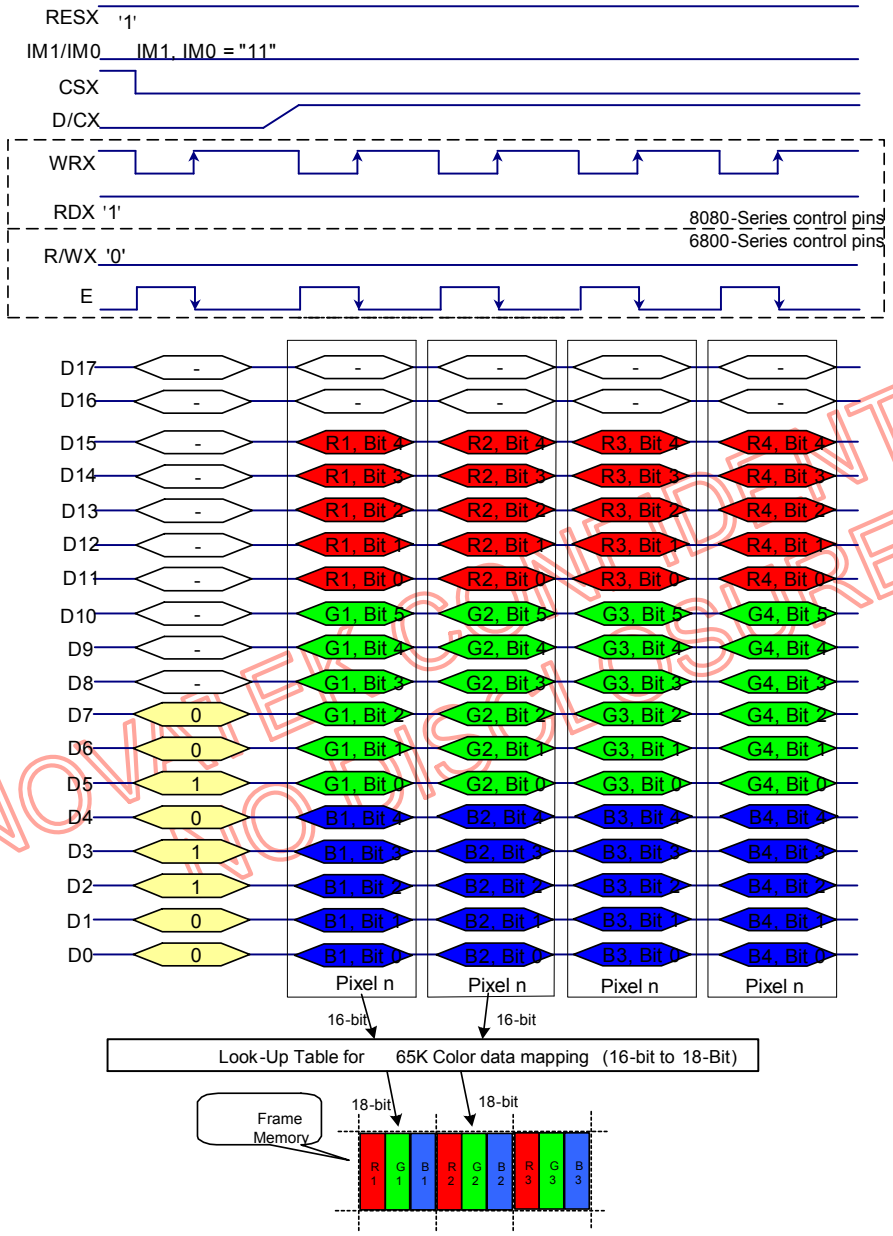


Note1. The data order is ad follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.
Note 2.1-times transfer is used to transmit 1 pixel data with the 12-bits color depth information.

Note 3. '-' = Don't care - Can be set to VDDI or DGND level

Write 18-bits data for RGB 5-6-5-bits input (65k-color)

There is 1 pixel (3 sub-pixels) per 1-transfer, 16-bits/pixel. 3AH="05h"



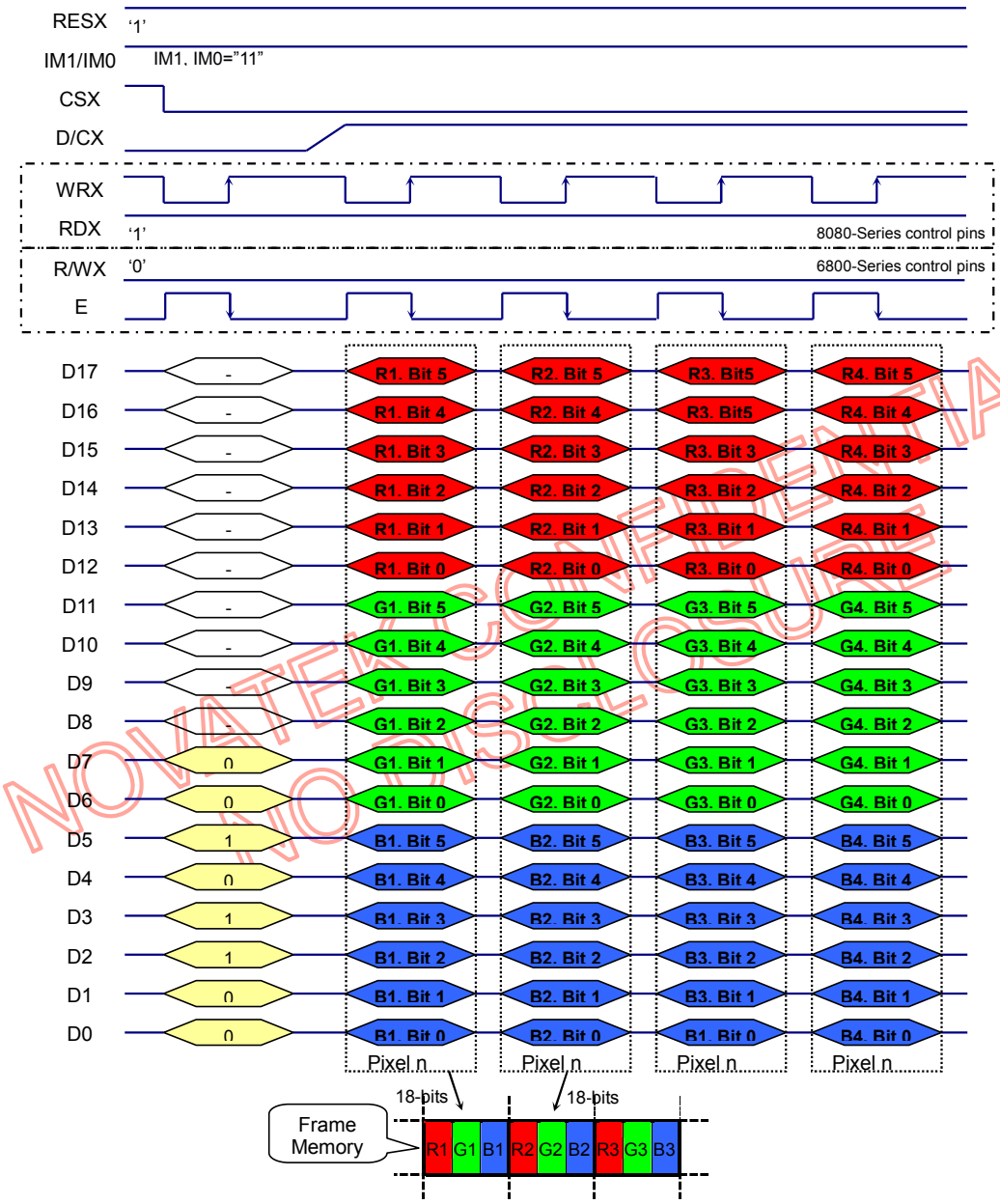
Note1. The data order is ad follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2.1-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.

Note 3. '-' = Don't care - Can be set to VDDI or DGND level

Write 18-bit data for RGB 6-6-6-bits input (262k-color)

There is 1 pixel (3 sub-pixels) per 1-transfer, 18-bit/pixel. 3AH="06h"



Note1. The data order is ad follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Read, Green and Blue data.

Note 2.1-times transfer (D17o D0) is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3. '-' = Don't care - Can be set to '0' or '1'

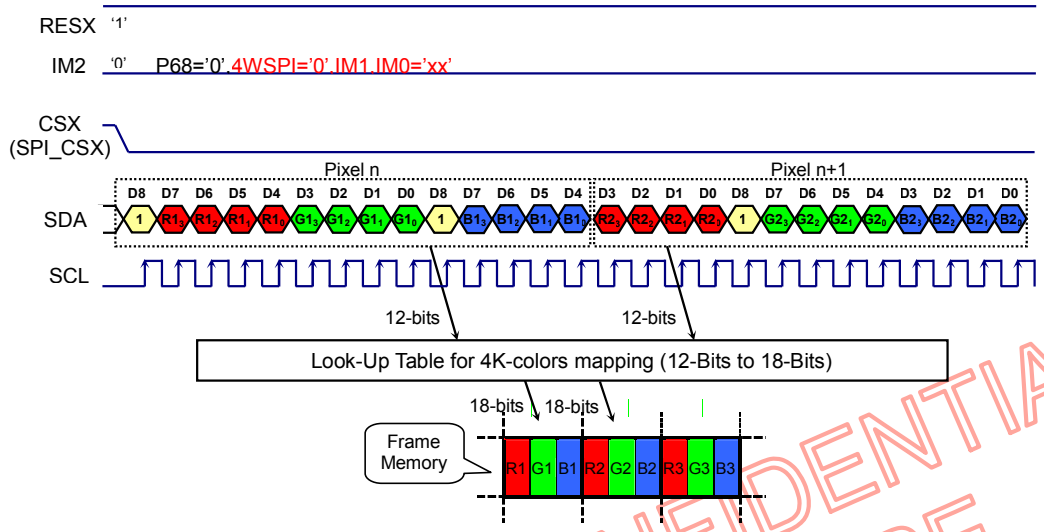
5.2.1.5 3-pins Serial Interface

Different display data formats are available for three Colors depth supported by listed below.

- 4k Colors, RGB 4,4,4-bits input, (3AH=”03h”)
- 65k Colors, RGB 5,6,5-bits input,(3AH=”05h”)
- 262k Colors, RGB 6,6,6-bits input, (3AH=”06h”)

Write data for RGB 4-4-4-bits input

3-pin 9-bit Series data protocol 3AH="03h"



Note 1. pixel data with the 12-bits color depth information

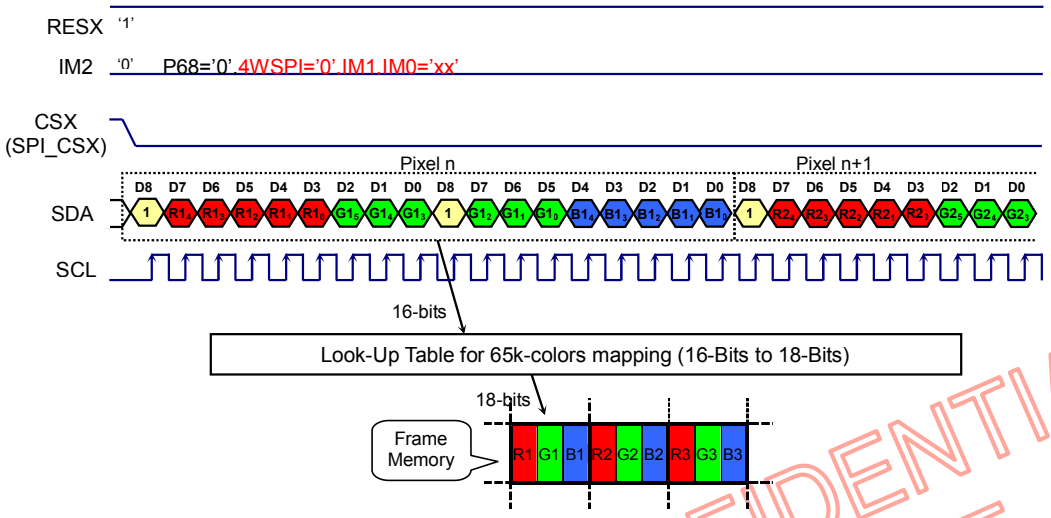
Note 2. The most significant bits are: Rx3, Gx3 and Bx3

Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Note 4. X = Don't care - Can be set to '0' or '1'

Write data for RGB 5-6-5-bits input

3-pin 9-bit Series data protocol 3AH="05h"



Note 1. pixel data with the 16-bit color depth information

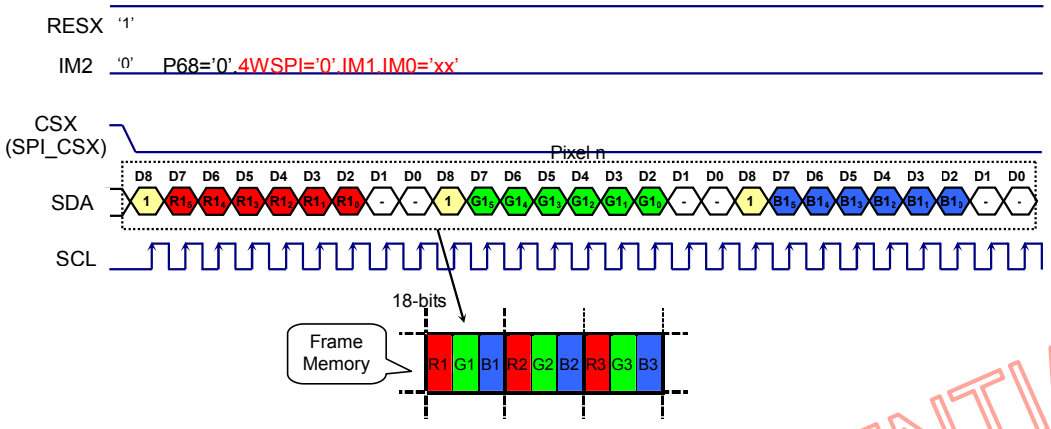
Note 2. The most significant bits are: Rx5, Gx5 and Bx5

Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Note 4. X = Don't care - Can be set to '0' or '1'

Write data for RGB 6-6-6-bits input

3-pin 9-bit Series data protocol 3AH="06h"



Note 1. pixel data with the 18-bit color depth information

Note 2. The most significant bits are: Rx5, Gx5 and Bx5

Note 3. The least significant bits are: Rx0, Gx0 and Bx0

ote 4. X = Don't care - Can be set to '0' or '1'

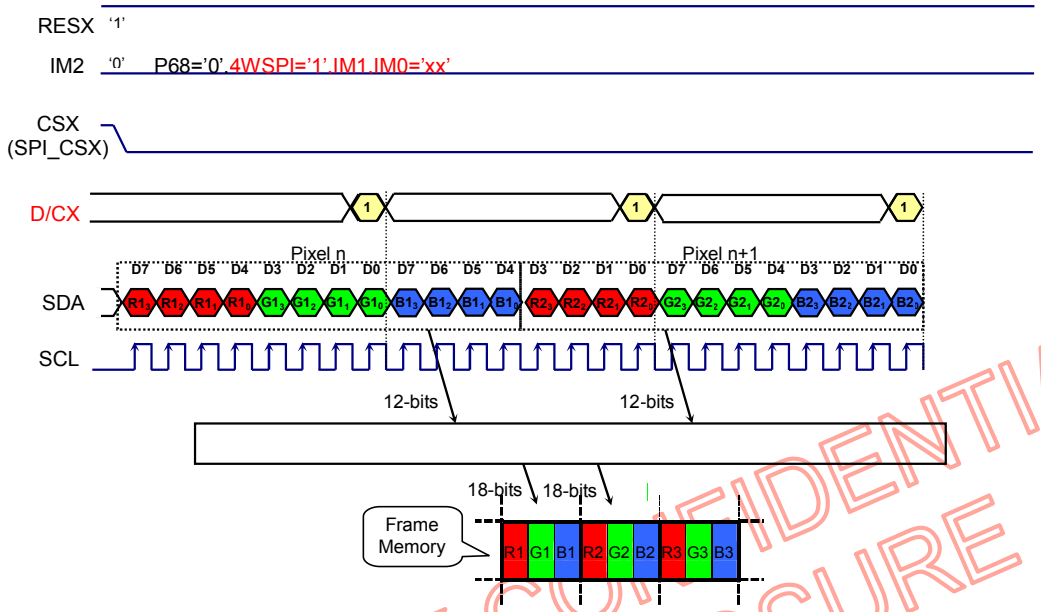
5.2.1.6 4-pins Serial Interface

Different display data formats are available for three Colors depth supported by listed below.

- 4k Colors, RGB 4,4,4-bits input, (3AH=”03h”)
- 65k Colors, RGB 5,6,5-bits input,(3AH=”05h”)
- 262k Colors, RGB 6,6,6-bits input, (3AH=”06h”)

Write data for RGB 4-4-4-bits input

4-pin 8-bit Series data protocol 3AH="03h"



Note 1. pixel data with the 12-bits color depth information

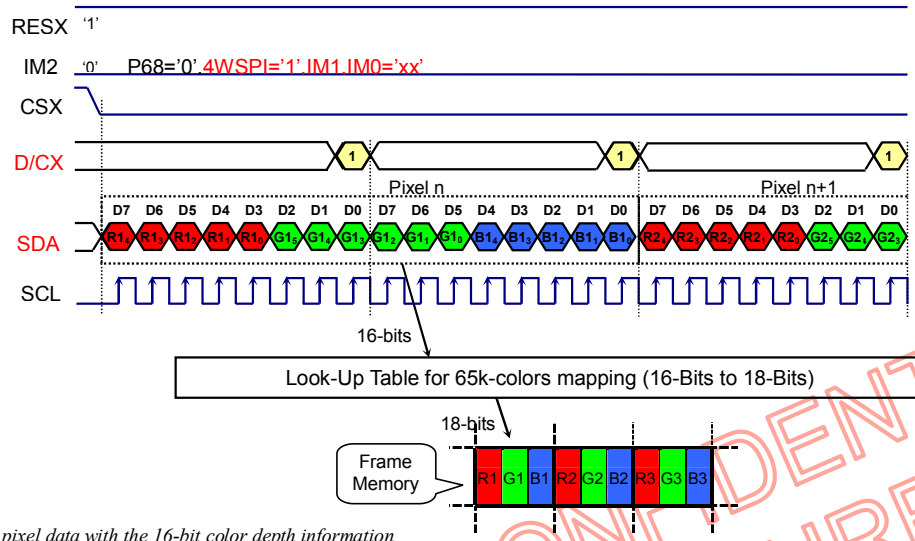
Note 2. The most significant bits are: Rx3, Gx3 and Bx3

Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Note 4. X = Don't care - Can be set to '0' or '1'

Write data for RGB 5-6-5-bits input

4-pin 8-bit Series data protocol 3AH=”05h”



Note 1. pixel data with the 16-bit color depth information

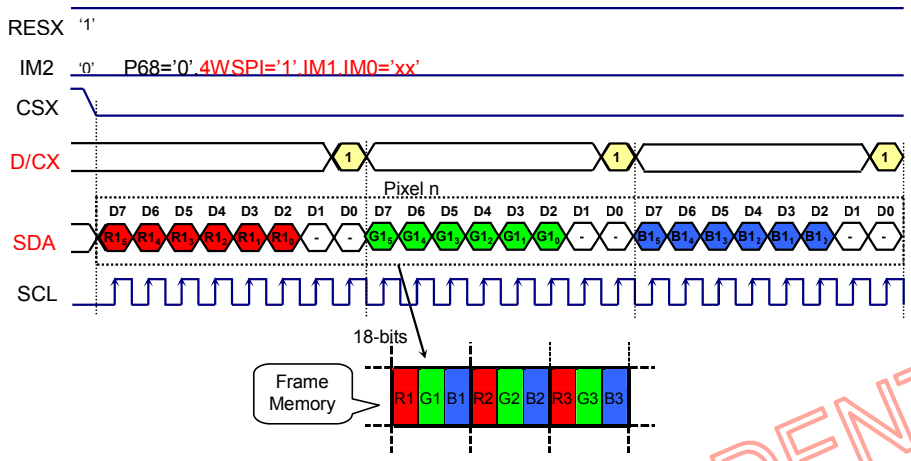
Note 2. The most significant bits are: Rx5, Gx5 and Bx5

Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Note 4. X = Don't care - Can be set to '0' or '1'

Write data for RGB 6-6-6-bits input

4-pin 8-bit Series data protocol 3AH="06h"



Note 1. pixel data with the 18-bit color depth information

Note 2. The most significant bits are: Rx5, Gx5 and Bx5

Note 3. The least significant bits are: Rx0, Gx0 and Bx0

ote 4. X = Don't care - Can be set to '0' or '1'

5.2.1.7 MCU data read format

8-Bits Parallel Interface

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	2Eh
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	X	x	262K-Colour (1-pixels/ 3byyes)
x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	X	x	
x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	X	x	

16-Bits Parallel Interface

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	2Eh
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	262K-Colour (2-pixels/ 3byyes)
x	x	B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x	
x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x	

9-Bits Parallel Interface

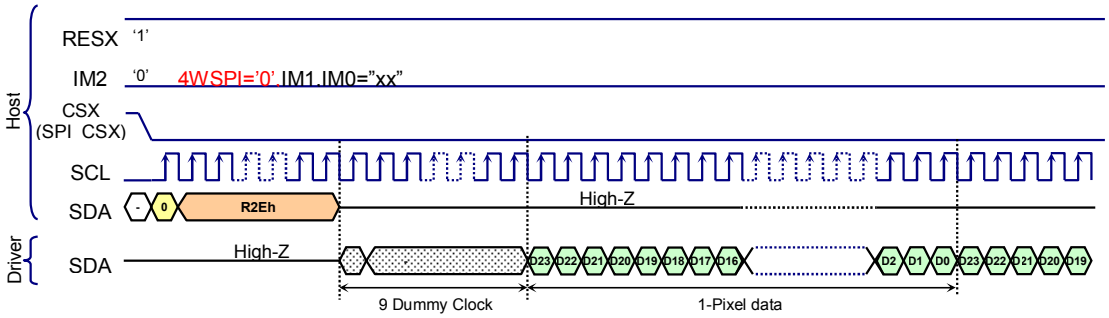
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	2Eh
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Colour (1-pixels/ 2byyes)
x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

18-Bits Parallel Interface

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	2Eh
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Colour

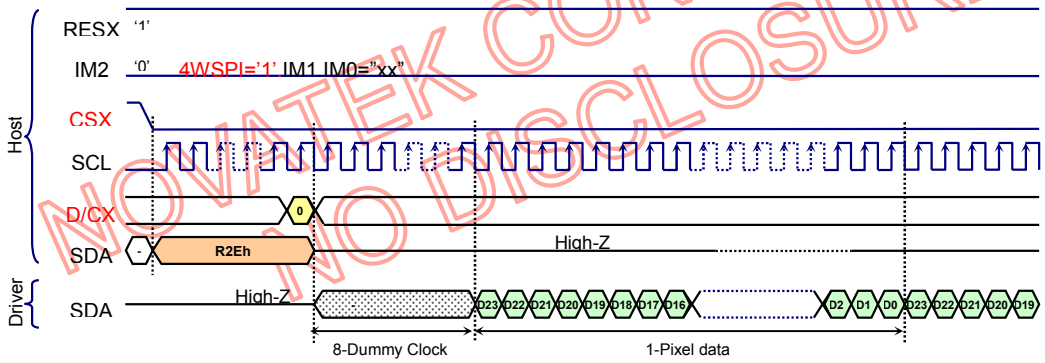
5.2.1.8 SPI data read format

3-pins Serial Interface



Read Data format as below

4-pins Serial Interface



Read Data format as below

5.2.2 RGB interface

5.2.2.1 General Description

The module uses 6, 16 and 18-bits parallel RGB interface which includes: VS, HS, DE, PCLK, D[17:0]. The interface is activated after Power On sequence (See section Power On/Off Sequence)

Pixel clock (PCLK) is running all the time without stopping and it is used to entering VS, HS, DE and D[17:0] states when there is a rising edge of the PCLK. The PCLK cannot be used as continues internal clock for other functions of the display module e.g. Sleep In–mode etc.

Vertical synchronization (VS) is used to tell when there is received a new frame of the display. This is negative (‘0’, low) active and its state is read to the display module by a rising edge of he PCLK signal.

Horizontal synchronization (HS) is used to tell when there is received a new line of the frame. This is negative (‘0’, low) active and its state is read to the display module by a rising edge of the PCLK signal.

Data Enable (DE) is used to tell when there is received a RGB information that should be transferred on the display. This is a positive (‘1’, high) active and its state is read to the display module by a rising edge of the PCLK signal.

D[17:0] (18-bit: R5-R0, G5-G0 and B5-B0; 16-bit: R4-R0, G5-G0 and B4-B0) are used to tell what is the information of the image that is transferred on the display (When DE=’1’ and there is a rising edge of PCLK). D[17:0] can be ‘0’ (low) or ‘1’ (high). These lines are read by a rising edge of the PCLK signal.

The PCLK cycle is described in the following figure.

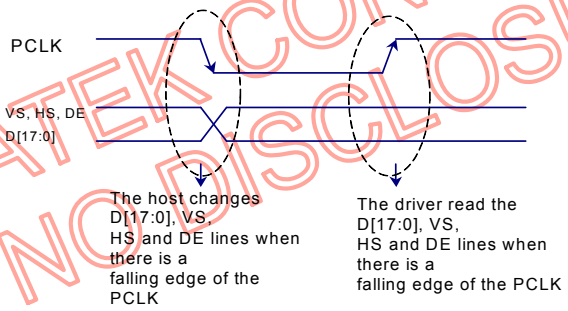


Fig. 5.2.2.1 PCLK cycle

Note: PCLK is an unsynchronized signal (It can be stopped).

5.2.2.2 RGB Interface Bus Width Set

All 4-kinds of bus width can be available during RGB interface mode (selected by COLMOD (3Ah) command for 8-bits, 16-bits and 18-bits data width)

VIPF[3:0]	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus width
0101	R4	R3	R2	R1	R0	x	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	x	16-bits data
0110	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	18-bits data
1110	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	6-bits data
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

Note 1: When VIPF[3:0]= 1110 , 6-bits data width of 3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Note 2: Only VIPF[3:0]= 0101 , 0110 and 1110 are valid on RGB I/F, Others are invalid.

Note 3. x Don t care, but need to set VDDI or DGND level.

5.2.2.3 RGB Interface Mode Set

Table 5.2.2.3 RGB Interface Mode Set

RGB I/F Mode	PCLK	DE	VS	HS	Video Data bus D[17:0]	Register for Blanking Porch setting	Reference clock for Display
RGB Mode 1	Used	Used	Used	Used	Used	Not Used	Internal Oscillator
RGB Mode 2	Used	Used	Used	Used	Used	Used	Internal Oscillator

There are 2-kinds of RGB mode which is selected by RCM1 & RCM0 hardware pins.

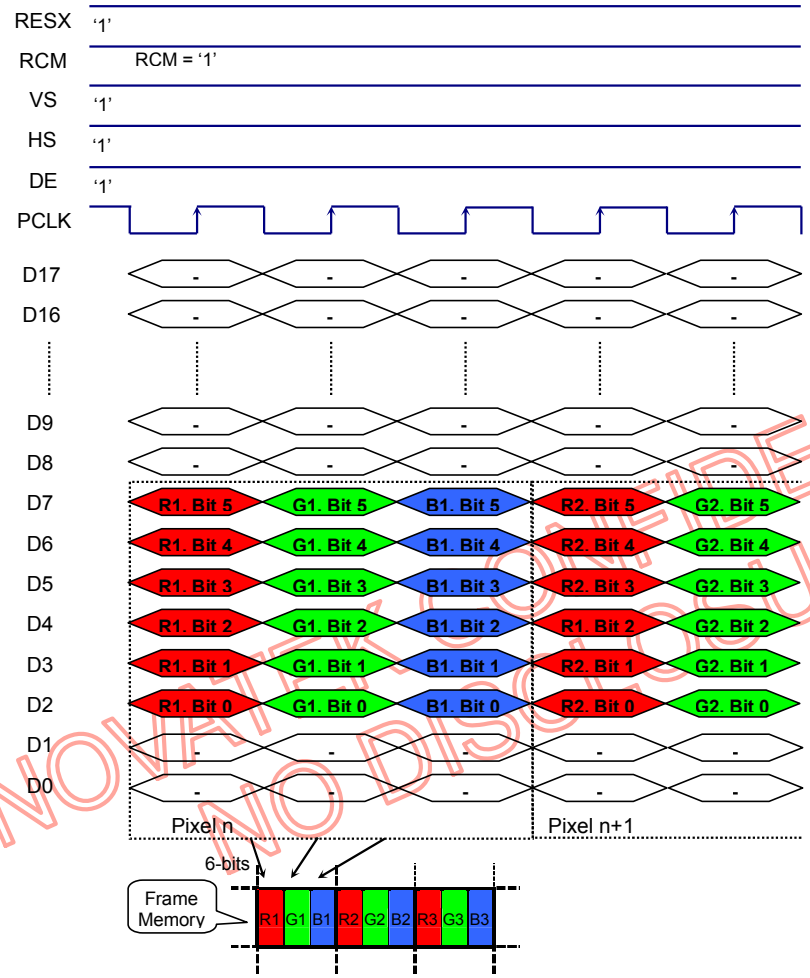
In RGB Mode 1 : (RCM1, RCM0 = "10"), writing data to frame memory is done by PCLK and Video Data Bus (D[23:0]), when DE is high state. The external synchronization signals (PCLK, VS and HS) are used for internal display signals. So, controller (host) must always transfer PCLK, VS, HS and DE signals to driver.

In RGB Mode 2 : (RCM1, RCM0 = "11"), blanking porch setting of VS and HS signals are defined by RGBBPCTR (B5h) command. DE pin is used for data making. When DE pin is high, valid data is directly stored to frame memory. In the contrast, if DE pin is low the data of frame memory will keep same status.

5.2.2.3 RGB Data color coding

18-bits/pixel Colors Order on 6-bits Data width RGB Interface (RGB 6-6-6-bits input)

There are 1 pixel (3 sub-pixels) per 3 bytes, 262K-colours, 3AH="F0h"

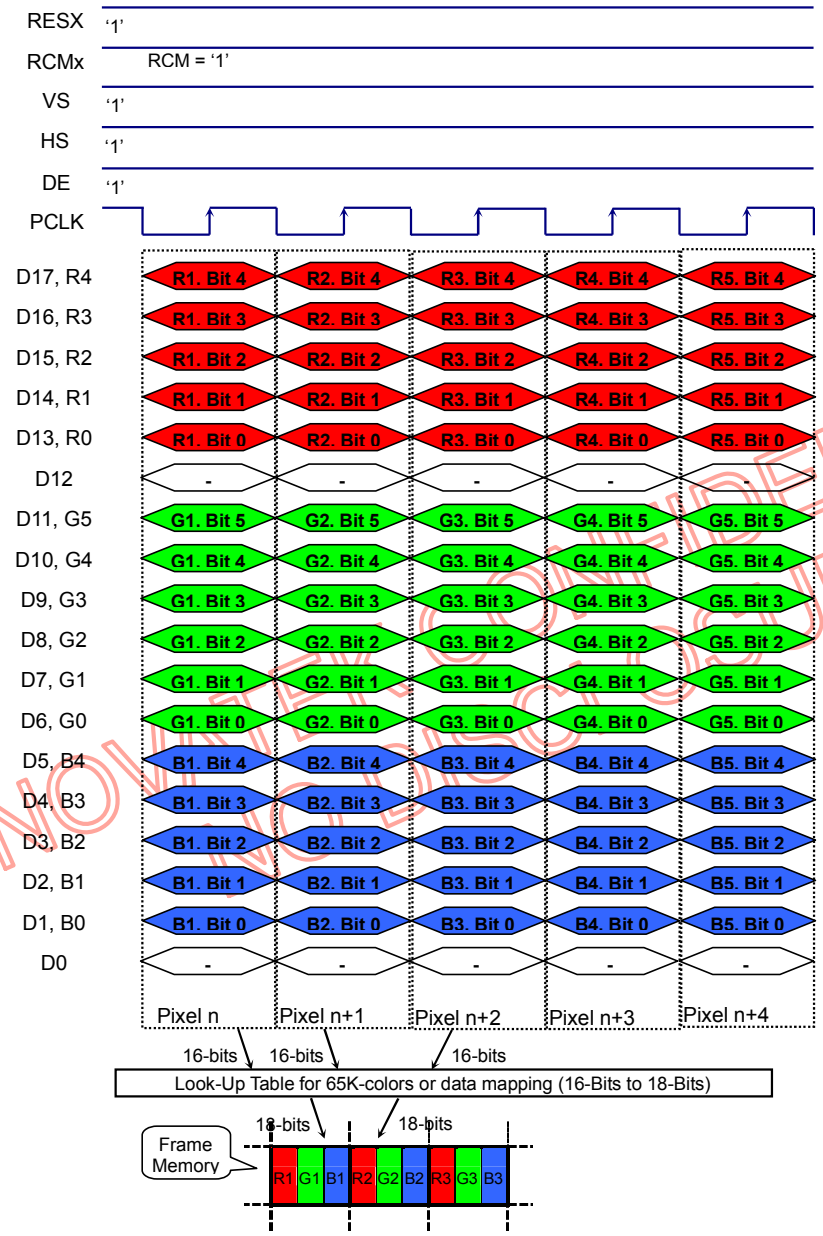


Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit7, LSB=Bit0 for Red, Green and Blue data. (3-trandfer data one pixel)

Note 2. '-' Don't care, but need to set VDDI or DGND level.

16-bits/pixel Colors Order on the 16-bits Data width RGB Interface (RGB 5-6-5-bits input)

There are 1 pixel (3 sub-pixels) per 1 bytes, 65K-colours, 3AH="50h"

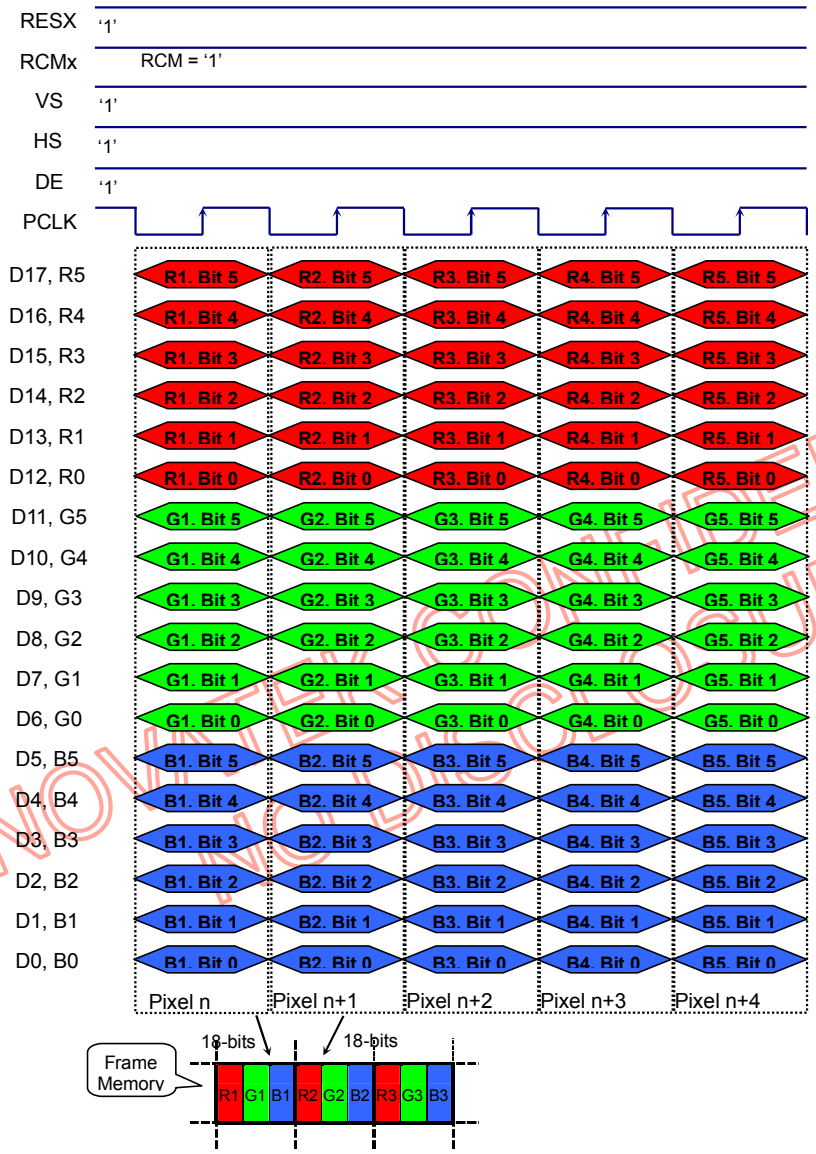


Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit5, LSB=Bit0 for Green data and MSB=Bit4, LSB=Bit0 for Red and Blue data.

Note 2. '-' Don't care, but need to set VDDI or DGND level.

18-bits/pixel Colors Order on the 18-bits Data width RGB Interface (RGB 6-6-6-bits input)

There are 1 pixel (3 sub-pixels) per 1 bytes, 262K-colours, 3AH="60h"



Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit5, LSB=Bit0 for Red, Green and Blue data.

Note 2. '-' Don't care, but need to set VDDI or DGND level.

5.2.3 Address Counter

The address counter sets the addresses of the display data RAM for writing and reading.

Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 6-6-6-bit), according to the data formats. As soon as this pixel-data information is complete the "Write access" is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=176 (AFh) and Y=0 to Y=220 (DBh). Addresses outside these ranges are not allowed. Before writing to the RAM a window must be defined into which will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=176 (AFh), YE=220 (DBh).

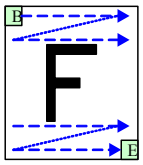
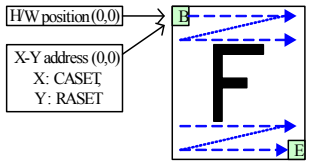
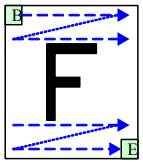
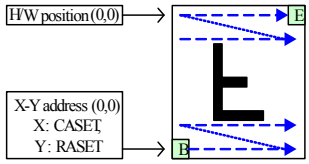
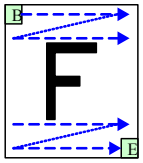
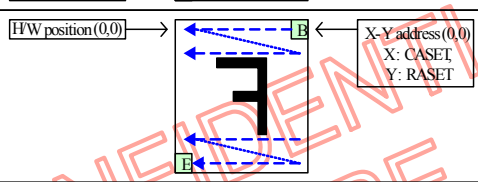
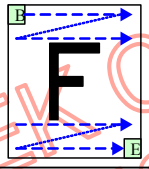
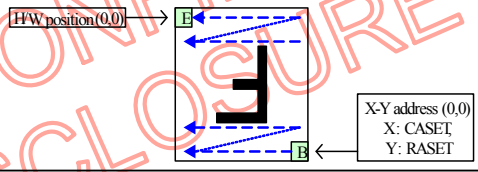
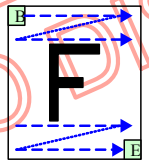
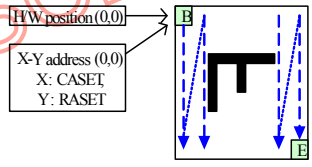
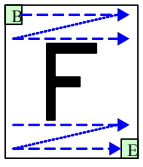
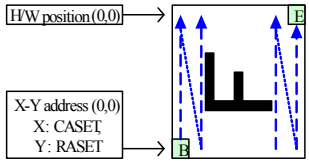
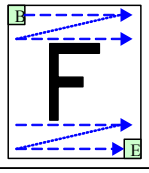
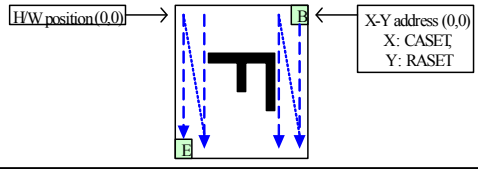
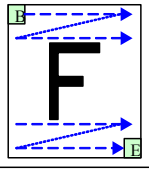
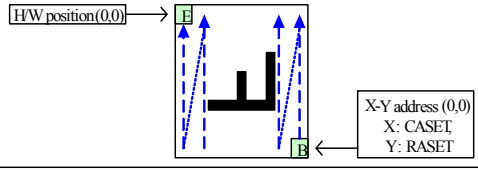
In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands "CASET, RASET" and "MADCTR" (see section 9 command list), define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Fig. 5.2.3 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data bust be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as Fig. 8.2.3 below:

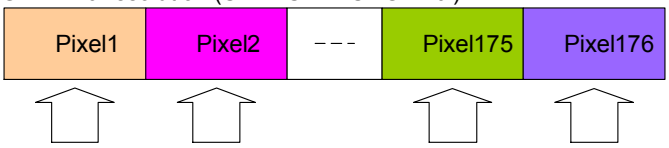
Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to "Start Column (XS)"	Return to "Start Row (YS)"
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than "End Column (XE)"	Return to "Start Column (XS)"	Increment by 1
The Column counter value is larger than "End Column (XE)" and the Row counter value is larger than "End Row (YE)"	Return to "Start Column (XS)"	Return to "Start Row (YS)"

Fig. 5.2.3 Frame Data Write Direction According to the MADCTR parameters (MV, MX and MY)

Display Data Direction	MADCTR Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y- Mirror	0	0	1		
X- Mirror	0	1	0		
X- Mirror Y- Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y- Mirror	1	0	1		
X-Y Exchange X- Mirror	1	1	0		
X- Y Exchange X- Mirror Y- Mirror	1	1	1		

5.2.4 Memory to Display Address Mapping

When using 176RGB x 220 resolution (SMX=SMY=SRGB='0')



Gate Out	Source Out		S1	S2	S3	S 4	S 5	S 6	– – –	S523	S524	S525	S526	S527	S528		
			RGB=0		RGB=1	RGB=0		RGB=1	RGB Order	RGB=0		RGB=1	RGB=0		RGB=1		
	RA															SA	
	MY=0	MY=1														ML=0	ML=1
1	1	220	R0	G0	B0	R1	G1	B1	– – –	R175	G175	B175	R176	G176	B176	1	220
2	2	219							– – –							2	219
3	3	218							– – –							3	218
4	4	217							– – –							4	217
5	5	216							– – –							5	216
6	6	215							– – –							6	215
7	7	214							– – –							7	214
8	8	213							– – –							8	213
9	9	212							– – –							9	212
10	10	211							– – –							10	211
11	11	210							– – –							11	210
12	12	209							– – –							12	209
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	– – –	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
213	213	8							– – –							213	8
214	214	7							– – –							214	7
215	215	6							– – –							215	6
216	216	5							– – –							216	5
217	217	4							– – –							217	4
218	218	3							– – –							218	3
219	219	2							– – –							219	2
220	220	1							– – –							220	1
	CA	MX=0	1			2			– – –	175			176				
		MX=1	176			175			– – –	2			1				

Note

RA = Row Address,

CA = Column Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Column address direction parameter), D7 parameter of MADCTL command

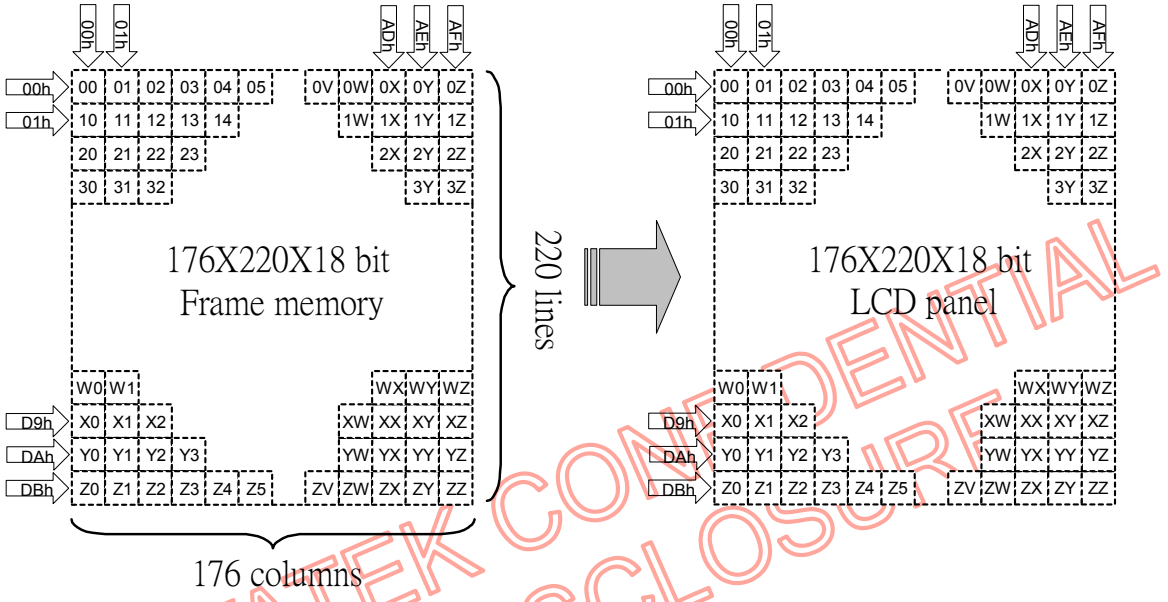
ML =Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

5.2.5 Normal Display On or Partial Mode On, Vertical Scroll Off

In this mode, contents of the frame memory within an area where column pointer is 00h to AFh and page pointer is 00h to DBh is displayed.

To display a dot on left most top corner, store the dot data at (column pointer, row pointer) = (0, 0).



5.2.6 Vertical Scroll Mode

5.2.6.1 Scrolling

There is vertical scrolling, which are determined by the commands "Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

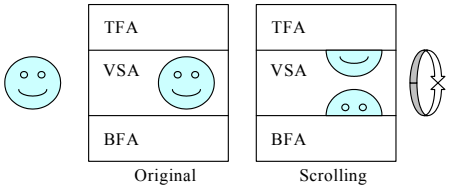
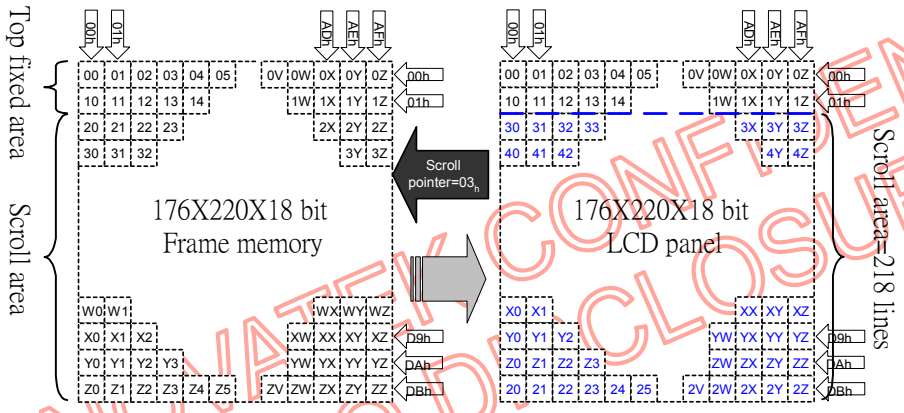


Fig. 5.2.6.1 Difference between Scrolling and original

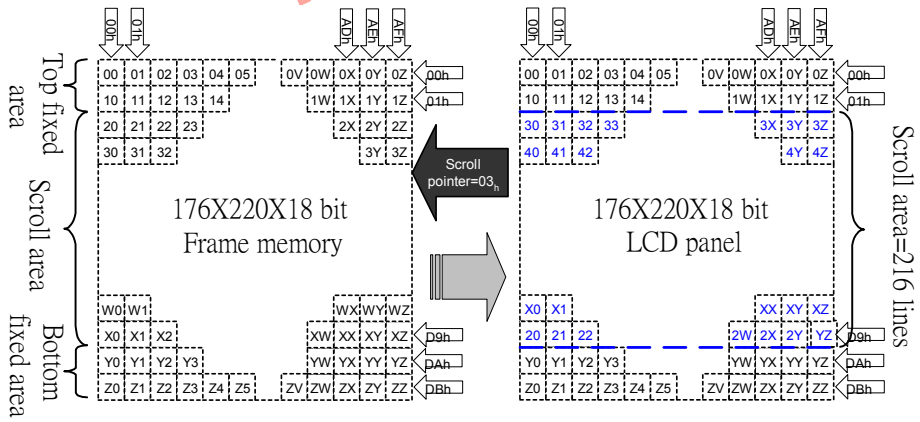
1). Example 1

TFA =2, VSA=218, BFA=0, when MADCTL Bit B4=0



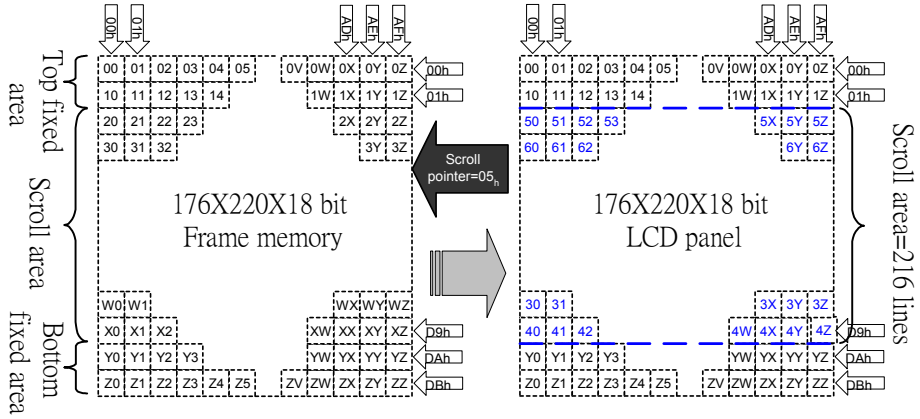
2). Example 2

TFA =2, VSA=216, BFA=2, when MADCTL Bit B4=0



3). Example 3

TFA =2, VSA=216, BFA=2, when MADCTL Bit B4=0



Note: When Vertical Scrolling Definition Parameter (TFA+VSA+BFA) ≠220,Scrolling Mode is undefined.

5.2.6.2 Vertical Scroll Example

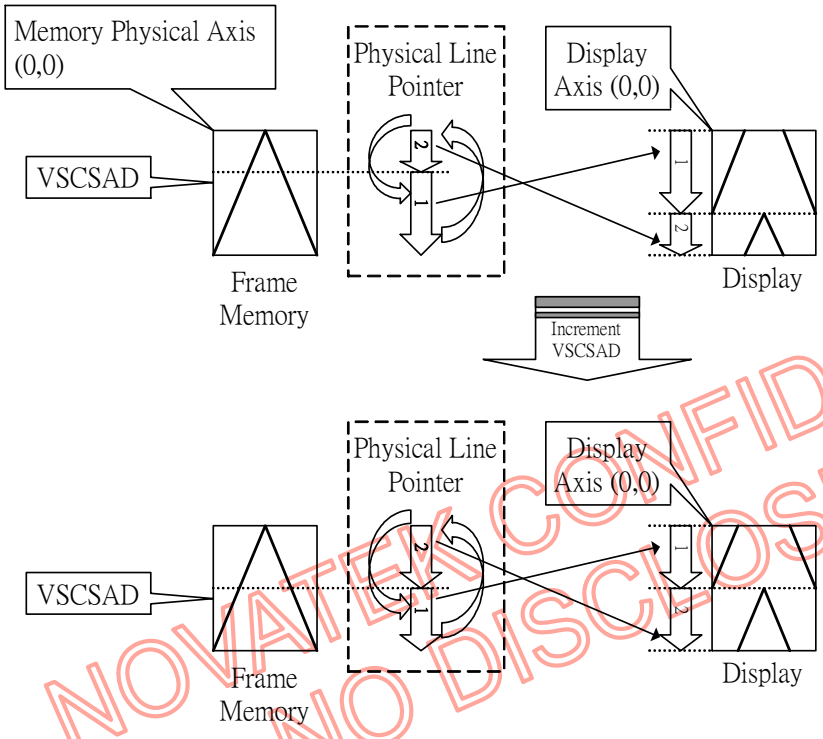
There are 2 types of vertical scrolling, which are determined by the commands " Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

Case 1: TFA + VSA + BFA＜220

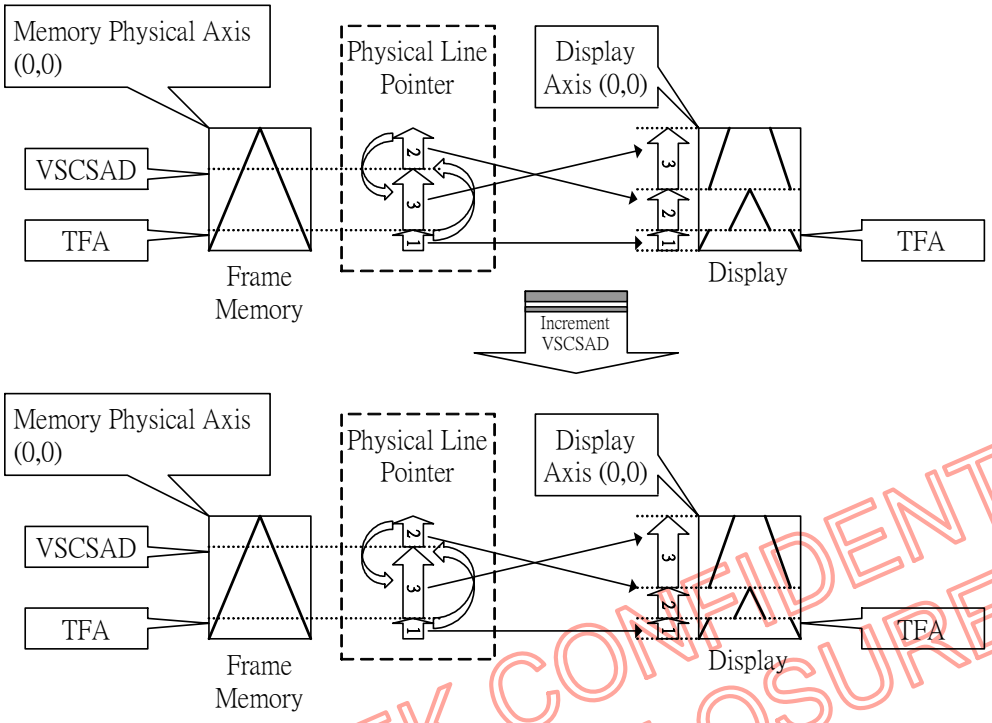
N/A. Do not set TFA + VSA + BFA＜220. In that case, unless unexpected picture will be shown.

Case 2: TFA + VSA + BFA=220 (Scrolling)

Example1) When MADCTR parameter ML="0",TFA=0, VSA=220, BFA=0 and VSCSAD=40.



Example2) When MADCTR parameter ML="1",TFA=30, VSA=190, BFA=0 and VSCSAD=80.

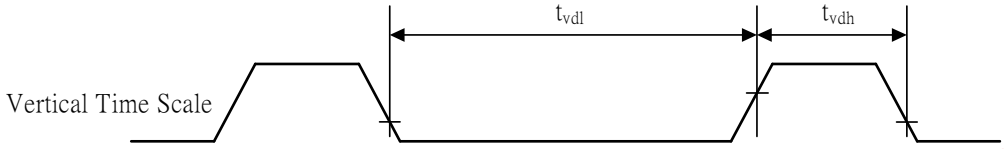


5.2.7 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

5.2.7.1 Tearing Effect Line Modes

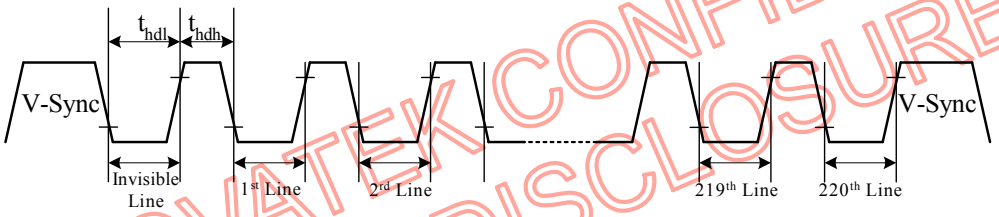
Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:



t_{vdh} = The LCD display is not updated from the Frame Memory

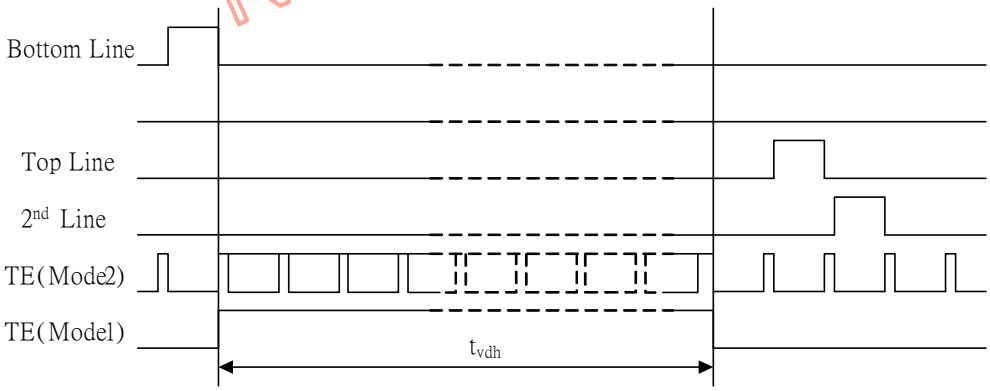
t_{vdl} = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 220 H-sync pulses per field.



t_{hdh} = The LCD display is not updated from the Frame Memory

t_{hdl} = The LCD display is updated from the Frame Memory (except Invisible Line – see above)



Note: During Sleep In Mode, the Tearing Output Pin is active Low.

5.2.7.2 Tearing Effect Line Timing

The Tearing Effect signal is described below:

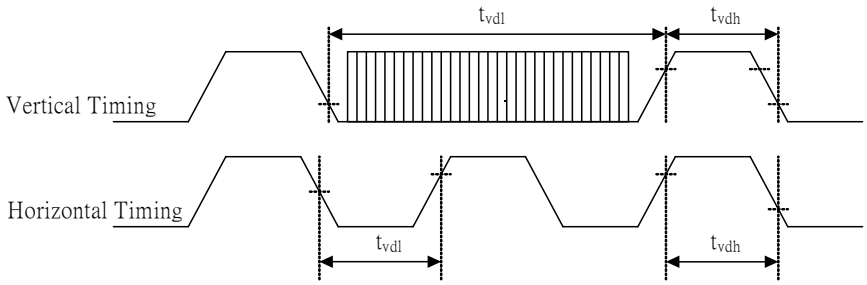


Table 5.2.7.2 AC characteristics of Tearing Effect Signal

Idle Mode Off (Frame Rate = 60.5 Hz)

Symbol	Parameter	min	max	unit	description
tvdl	Vertical Timing Low Duration	13	-	ms	
tvdh	Vertical Timing High Duration	1000	-	μs	
thdl	Horizontal Timing Low Duration	33	-	μs	
thdh	Horizontal Timing High Duration	25	500	μs	

NOTE: The timings in Table 5.2.7.2 apply when MADCTR ML=0 and ML=1

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

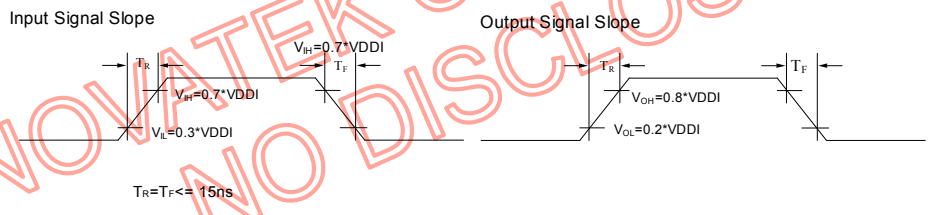
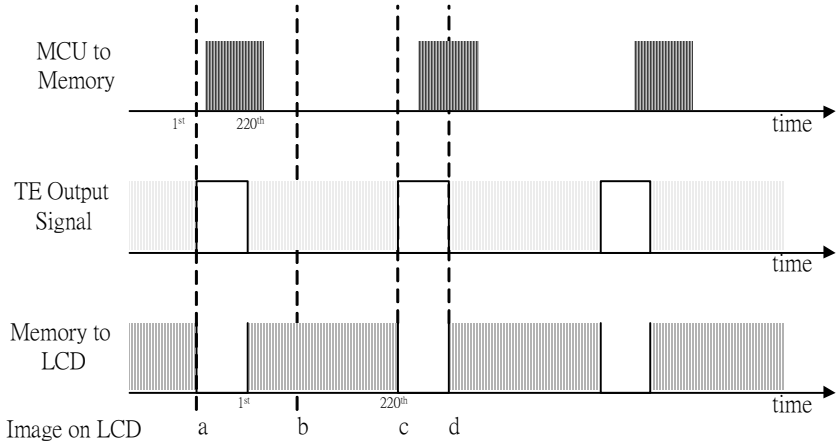


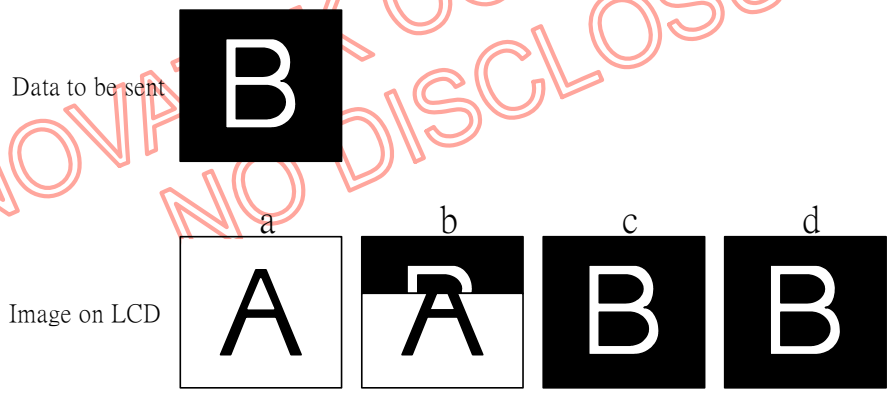
Fig. 7.1.2 Rising and Falling timing for Input and Output signal

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

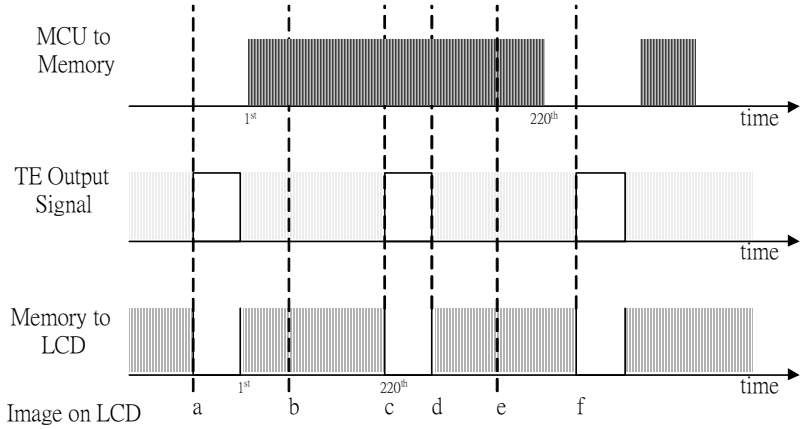
5.2.7.3 Example 1: MPU Write is faster than panel read.



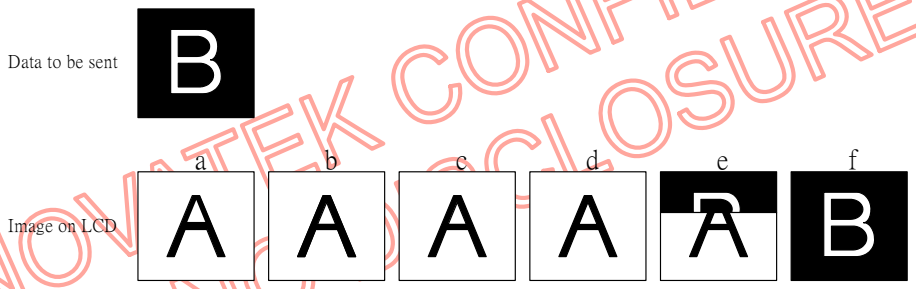
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



5.2.7.4 Example 2: MPU Write is Slower than panel read.



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer "catches" the MPU to Frame memory write position.



5.2.8 Color Depth Conversion Look Up Tables

4096 and 65536 Color to 262,144 Color

(After H/W reset or Power ON, the default value is RGB 5-6-5 to RGB 6-6-6)

Color	Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W Reset	RGBSET parameter	Look Up Table Input Data	
				4k Color	65k Color
RED	R_{005} R_{004} R_{003} R_{002} R_{001} R_{000}	000000	1	0000	00000
	R_{015} R_{014} R_{013} R_{012} R_{011} R_{010}	000011	2	0001	00001
	R_{025} R_{024} R_{023} R_{022} R_{021} R_{020}	000101	3	0010	00010
	R_{035} R_{034} R_{033} R_{032} R_{031} R_{030}	000111	4	0011	00011
	R_{045} R_{044} R_{043} R_{042} R_{041} R_{040}	001001	5	0100	00100
	R_{055} R_{054} R_{053} R_{052} R_{051} R_{050}	001011	6	0101	00101
	R_{065} R_{064} R_{063} R_{062} R_{061} R_{060}	001101	7	0110	00110
	R_{075} R_{074} R_{073} R_{072} R_{071} R_{070}	001111	8	0111	00111
	R_{085} R_{084} R_{083} R_{082} R_{081} R_{080}	010001	9	1000	01000
	R_{095} R_{094} R_{093} R_{092} R_{091} R_{090}	010011	10	1001	01001
	R_{105} R_{104} R_{103} R_{102} R_{101} R_{100}	010101	11	1010	01010
	R_{115} R_{114} R_{113} R_{112} R_{111} R_{110}	010111	12	1011	01011
	R_{125} R_{124} R_{123} R_{122} R_{121} R_{120}	011001	13	1100	01100
	R_{135} R_{134} R_{133} R_{132} R_{131} R_{130}	011011	14	1101	01101
	R_{145} R_{144} R_{143} R_{142} R_{141} R_{140}	011101	15	1110	01110
	R_{155} R_{154} R_{153} R_{152} R_{151} R_{150}	011111	16	1111	01111
	R_{165} R_{164} R_{163} R_{162} R_{161} R_{160}	100001	17	Not	10000
	R_{175} R_{174} R_{173} R_{172} R_{171} R_{170}	100011	18	Used	10001
	R_{185} R_{184} R_{183} R_{182} R_{181} R_{180}	100101	19		10010
	R_{195} R_{194} R_{193} R_{192} R_{191} R_{190}	100111	20		10011
	R_{205} R_{204} R_{203} R_{202} R_{201} R_{200}	101001	21		10100
	R_{215} R_{214} R_{213} R_{212} R_{211} R_{210}	101011	22		10101
	R_{225} R_{224} R_{223} R_{222} R_{221} R_{220}	101101	23		10110
	R_{235} R_{234} R_{233} R_{232} R_{231} R_{230}	101111	24		10111
	R_{245} R_{244} R_{243} R_{242} R_{241} R_{240}	110001	25		11000
	R_{255} R_{254} R_{253} R_{252} R_{251} R_{250}	110011	26		11001
	R_{265} R_{264} R_{263} R_{262} R_{261} R_{260}	110101	27		11010
	R_{275} R_{274} R_{273} R_{272} R_{271} R_{270}	110111	28		11011
	R_{285} R_{284} R_{283} R_{282} R_{281} R_{280}	111001	29		11100
	R_{295} R_{294} R_{293} R_{292} R_{291} R_{290}	111011	30		11101
	R_{305} R_{304} R_{303} R_{302} R_{301} R_{300}	111101	31		11110
	R_{315} R_{314} R_{313} R_{312} R_{311} R_{310}	111111	32		11111

Color	Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W Reset	RGBSET parameter	Look Up Table Input Data	
				4k Color	65K Color
GREEN	G_{005} $G_{004}G_{003}G_{002}G_{001}G_{000}$	000000	33	0000	000000
	$G_{015}G_{014}G_{013}G_{012}G_{011}G_{010}$	000001	34	0001	000001
	$G_{025}G_{024}G_{023}G_{022}G_{021}G_{020}$	000010	35	0010	000010
	$G_{035}G_{034}G_{033}G_{032}G_{031}G_{030}$	000011	36	0011	000011
	$G_{045}G_{044}G_{043}G_{042}G_{041}G_{040}$	000100	37	0100	000100
	$G_{055}G_{054}G_{053}G_{052}G_{051}G_{050}$	000101	38	0101	000101
	$G_{065}G_{064}G_{063}G_{062}G_{061}G_{060}$	000110	39	0110	000110
	$G_{075}G_{074}G_{073}G_{072}G_{071}G_{070}$	000111	40	0111	000111
	$G_{085}G_{084}G_{083}G_{082}G_{081}G_{080}$	001000	41	1000	001000
	$G_{095}G_{094}G_{093}G_{092}G_{091}G_{090}$	001001	42	1001	001001
	$G_{105}G_{104}G_{103}G_{102}G_{101}G_{100}$	001010	43	1010	001010
	$G_{115}G_{114}G_{113}G_{112}G_{111}G_{110}$	001011	44	1011	001011
	$G_{125}G_{124}G_{123}G_{122}G_{121}G_{120}$	001100	45	1100	001100
	$G_{135}G_{134}G_{133}G_{132}G_{131}G_{130}$	001101	46	1101	001101
	$G_{145}G_{144}G_{143}G_{142}G_{141}G_{140}$	001110	47	1110	001110
	$G_{155}G_{154}G_{153}G_{152}G_{151}G_{150}$	001111	48	1111	001111
	G_{165} $G_{164}G_{163}G_{162}G_{161}G_{160}$	010000	49	Not Used	010000
	$G_{175}G_{174}G_{173}G_{172}G_{171}G_{170}$	010001	50		010001
	$G_{185}G_{184}G_{183}G_{182}G_{181}G_{180}$	010010	51		010010
	$G_{195}G_{194}G_{193}G_{192}G_{191}G_{190}$	010011	52		010011
	$G_{205}G_{204}G_{203}G_{202}G_{201}G_{200}$	010100	53		010100
	$G_{215}G_{214}G_{213}G_{212}G_{211}G_{210}$	010101	54		010101
	$G_{225}G_{224}G_{223}G_{222}G_{221}G_{220}$	010110	55		010110
	$G_{235}G_{234}G_{233}G_{232}G_{231}G_{230}$	010111	56		010111
	$G_{245}G_{244}G_{243}G_{242}G_{241}G_{240}$	011000	57		011000
	$G_{255}G_{254}G_{253}G_{252}G_{251}G_{250}$	011001	58		011001
	$G_{265}G_{264}G_{263}G_{262}G_{261}G_{260}$	011010	59		011010
	$G_{275}G_{274}G_{273}G_{272}G_{271}G_{270}$	011011	60		011011
	$G_{285}G_{284}G_{283}G_{282}G_{281}G_{280}$	011100	61		011100
	$G_{295}G_{294}G_{293}G_{292}G_{291}G_{290}$	011101	62		011101
	$G_{305}G_{304}G_{303}G_{302}G_{301}G_{300}$	011110	63		011110
	$G_{315}G_{314}G_{313}G_{312}G_{311}G_{310}$	011111	64		011111

Color	Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W Reset	RGBSET parameter	Look Up Table Input Data	
				4k Color	65K Color
GREEN	G_{325} $G_{324}G_{323}G_{322}G_{321}G_{320}$	100000	65	Not Used	100000
	$G_{335}G_{334}G_{333}G_{332}G_{331}G_{330}$	100001	66		100001
	$G_{345}G_{344}G_{343}G_{342}G_{341}G_{340}$	100010	67		100010
	$G_{355}G_{354}G_{353}G_{352}G_{351}G_{350}$	100011	68		100011
	$G_{365}G_{364}G_{363}G_{362}G_{361}G_{360}$	100100	69		100100
	$G_{375}G_{374}G_{373}G_{372}G_{371}G_{370}$	100101	70		100101
	$G_{385}G_{384}G_{383}G_{382}G_{381}G_{380}$	100110	71		100110
	$G_{395}G_{394}G_{393}G_{392}G_{391}G_{390}$	100111	72		100111
	$G_{405}G_{404}G_{403}G_{402}G_{401}G_{400}$	101000	73		101000
	$G_{415}G_{414}G_{413}G_{412}G_{411}G_{410}$	101001	74		101001
	$G_{425}G_{424}G_{423}G_{422}G_{421}G_{420}$	101010	75		101010
	$G_{435}G_{434}G_{433}G_{432}G_{431}G_{430}$	101011	76		101011
	$G_{445}G_{444}G_{443}G_{442}G_{441}G_{440}$	101100	77		101100
	$G_{455}G_{454}G_{453}G_{452}G_{451}G_{450}$	101101	78		101101
	$G_{465}G_{464}G_{463}G_{462}G_{461}G_{460}$	101110	79		101110
	$G_{475}G_{474}G_{473}G_{472}G_{471}G_{470}$	101111	80		101111
	G_{485} $G_{484}G_{483}G_{482}G_{481}G_{480}$	110000	81		110000
	$G_{495}G_{494}G_{493}G_{492}G_{491}G_{490}$	110001	82		110001
	$G_{505}G_{504}G_{503}G_{502}G_{501}G_{500}$	110010	83		110010
	$G_{515}G_{514}G_{513}G_{512}G_{511}G_{510}$	110011	84		110011
	$G_{525}G_{524}G_{523}G_{522}G_{521}G_{520}$	110100	85		110100
	$G_{535}G_{534}G_{533}G_{532}G_{531}G_{530}$	110101	86		110101
	$G_{545}G_{544}G_{543}G_{542}G_{541}G_{540}$	110110	87		110110
	$G_{555}G_{554}G_{553}G_{552}G_{551}G_{550}$	110111	88		110111
	$G_{565}G_{564}G_{563}G_{562}G_{561}G_{560}$	111000	89		111000
	$G_{575}G_{574}G_{573}G_{572}G_{571}G_{570}$	111001	90		111001
	$G_{585}G_{584}G_{583}G_{582}G_{581}G_{580}$	111010	91		111010
	$G_{595}G_{594}G_{593}G_{592}G_{591}G_{590}$	111011	92		111011
	$G_{605}G_{604}G_{603}G_{602}G_{601}G_{600}$	111100	93		111100
	$G_{615}G_{614}G_{613}G_{612}G_{611}G_{610}$	111101	94		111101
	$G_{625}G_{624}G_{623}G_{622}G_{621}G_{620}$	111110	95		111110
	$G_{635}G_{634}G_{633}G_{632}G_{631}G_{630}$	111111	96		111111

Color	Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W Reset	RGBSET parameter	Look Up Table Input Data	
				4k Color	65K Color
BULE	B_{005} $B_{004}B_{003}B_{002}B_{001}B_{000}$	000000	97	0000	00000
	$B_{015}B_{014}B_{013}B_{012}B_{011}B_{010}$	000011	98	0001	00001
	$B_{025}B_{024}B_{023}B_{022}B_{021}B_{020}$	000101	99	0010	00010
	$B_{035}B_{034}B_{033}B_{032}B_{031}B_{030}$	000111	100	0011	00011
	$B_{045}B_{044}B_{043}B_{042}B_{041}B_{040}$	001001	101	0100	00100
	$B_{055}B_{054}B_{053}B_{052}B_{051}B_{050}$	001011	102	0101	00101
	$B_{065}B_{064}B_{063}B_{062}B_{061}B_{060}$	001101	103	0110	00110
	$B_{075}B_{074}B_{073}B_{072}B_{071}B_{070}$	001111	104	0111	00111
	$B_{085}B_{084}B_{083}B_{082}B_{081}B_{080}$	010001	105	1000	01000
	$B_{095}B_{094}B_{093}B_{092}B_{091}B_{090}$	010011	106	1001	01001
	$B_{105}B_{104}B_{103}B_{102}B_{101}B_{100}$	010101	107	1010	01010
	$B_{115}B_{114}B_{113}B_{112}B_{111}B_{110}$	010111	108	1011	01011
	$B_{125}B_{124}B_{123}B_{122}B_{121}B_{120}$	011001	109	1100	01100
	$B_{135}B_{134}B_{133}B_{132}B_{131}B_{130}$	011011	110	1101	01101
	$B_{145}B_{144}B_{143}B_{142}B_{141}B_{140}$	011101	111	1110	01110
	$B_{155}B_{154}B_{153}B_{152}B_{151}B_{150}$	011111	112	1111	01111
	B_{165} $B_{164}B_{163}B_{162}B_{161}B_{160}$	100001	113	Not Used	10000
	$B_{175}B_{174}B_{173}B_{172}B_{171}B_{170}$	100011	114		10001
	$B_{185}B_{184}B_{183}B_{182}B_{181}B_{180}$	100101	115		10010
	$B_{195}B_{194}B_{193}B_{192}B_{191}B_{190}$	100111	116		10011
	$B_{205}B_{204}B_{203}B_{202}B_{201}B_{200}$	101001	117		10100
	$B_{215}B_{214}B_{213}B_{212}B_{211}B_{210}$	101011	118		10101
	$B_{225}B_{224}B_{223}B_{222}B_{221}B_{220}$	101101	119		10110
	$B_{235}B_{234}B_{233}B_{232}B_{231}B_{230}$	101111	120		10111
	$B_{245}B_{244}B_{243}B_{242}B_{241}B_{240}$	110001	121		11000
	$B_{255}B_{254}B_{253}B_{252}B_{251}B_{250}$	110011	122		11001
	$B_{265}B_{264}B_{263}B_{262}B_{261}B_{260}$	110101	123		11010
	$B_{275}B_{274}B_{273}B_{272}B_{271}B_{270}$	110111	124		11011
	$B_{285}B_{284}B_{283}B_{282}B_{281}B_{280}$	111001	125		11100
	$B_{295}B_{294}B_{293}B_{292}B_{291}B_{290}$	111011	126		11101
	$B_{305}B_{304}B_{303}B_{302}B_{301}B_{300}$	111101	127		11110
	$B_{315}B_{314}B_{313}B_{312}B_{311}B_{310}$	111111	128		11111

5.3 MCU and RGB Interface Comparisons

Function	RCM1, RCM0				RCM1, RCM0			
Mode selection 1	"00"		"01"		"10"		"11"	
	8080/ 6800 IF + SPI I/F				RGB I/F + SPI I/F			
	MCU Mode 1		MCU Mode 2		RGB Mode 1		RGB Mode 2	
Mode selection 2	IM2='1'	IM2='0'	IM2='1'	IM2='0'	ICM='0'	ICM='1'	ICM='0'	ICM='1'
	8080/ 6800 IF	SPI I/F	8080/ 6800 IF	SPI I/F	RGB-1 I/F + SPI I/F		RGB-2 I/F + SPI I/F	
Motion /Still	Motion or	Still	Motion or	Still	Motion or	Still	Motion or Still	Still
Input data	D[17:0]	D0(SDA)	D[17:0]	SDA H/W pin	D[17:0]	SDA H/W pin	D[17:0]	SDA H/W pin
Input signal	WRX (R/WX),	WRX=SPI_DCX D/CX = SCL	WRX (R/WX),	WRX=SPI_DCX SCL H/W pin	PCLK	WRX=SPI_DCX D/CX = SCL	PCLK	WRX=SPI_DCX D/CX = SCL
	CSX	CSX	CSX	SPI_CSX	VS, HS, DE	CSX	VS, HS, DE	CSX
GRAM Write	Refer WRX	Refer SCL	Refer WRX	Refer SCL	Refer PCLK	Refer SCL	Refer PCLK	Refer SCL
GRAM Read	Refer Internal Oscillator				Refer PCLK	Refer Internal	Refer PCLK	Refer Internal
Command setting	D[7:0]	D0(SDA)	D[7:0]	SDA H/W pin	SDA H/W pin	SDA H/W pin	SDA H/W pin	SDA H/W pin
SMX, SMY,	-If those register not change, those H/W pins are always valid. If those registers be changed, should be follow registers setting.							
VSYNC Function	Default off		Default on		-Don't care in this mode.			
TE	Default off		Default on		Default off			
Normal / Partial	-By command setting							
Idle Mode	-By command setting						-By IDM H/W pin	
Display On/Off	-Don't care in this mode, but should be set to VDDI or DGND						-By SHUT H/W pin	
Data inverter							-By REV H/W pin	
DE H/W pin	-Don't care in this mode. But should be set to VDDI or DGND.				-The data latched by rising edge		-When DE='0' area, the data of	
RL H/W pin					-Don't care in this mode,but should be set to VDDI or		-By H/W pin	
TB H/W pin							-No commands conflict	
Blanking porch	-Don't care in this mode.				-Control by DE signal		-Control by RGBBPCTR (B5h)	
Colors format	-Control by IFPF[2:0] of COLMOD(3Ah)				-Control by VIPF[3:0] of COLMOD(3Ah)			

Note 1: RCM1 and RCM0 are H/W setting pins.

Note 2: In RGB + SPI I/F (RCM="1x"), VS, HS, DE, PCLK and D[17:0] are Hi-Z by Driver and can be stop for Host, when ICM='1'.

Note 3: In RGB + SPI I/F (RCM="1x"), the data deliver via GRAM

Note 4: When Power on Driver IC should be detect SMX, SMY, SRGB H/W setting

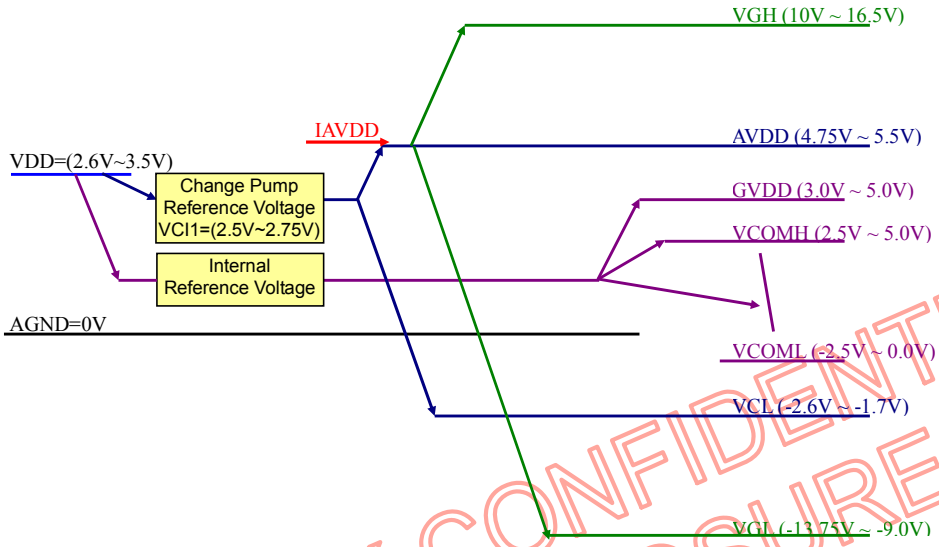
Note 5: When Power on Driver IC should be detect RCM1, RCM0 H/W setting and get into the I/F mode.

Note 6: When Power on Driver IC should be detect LCM1, LCM0 H/W setting and get into the setting mode.

Note 7: When Power on Driver IC should be detect GM1, GM0 H/W setting and get into the setting mode.

5.4 Power structure

5.4.1 LCD Power Generation Scheme



Remark

1. AVDD supply to all power source (exclude VGH, VGL)
2. Source output range: 0.1V ~ AVDD-0.1V
3. Linear Range: 0.2V ~ AVDD-0.2V
   (For all output voltage, but exclude VGH, VGL)
4. Above operating voltages is min range.
5. When VCI1=2.5V, the AVDD=4.75V (Min)

5.4.2 VCI1 generate from VDD regulator

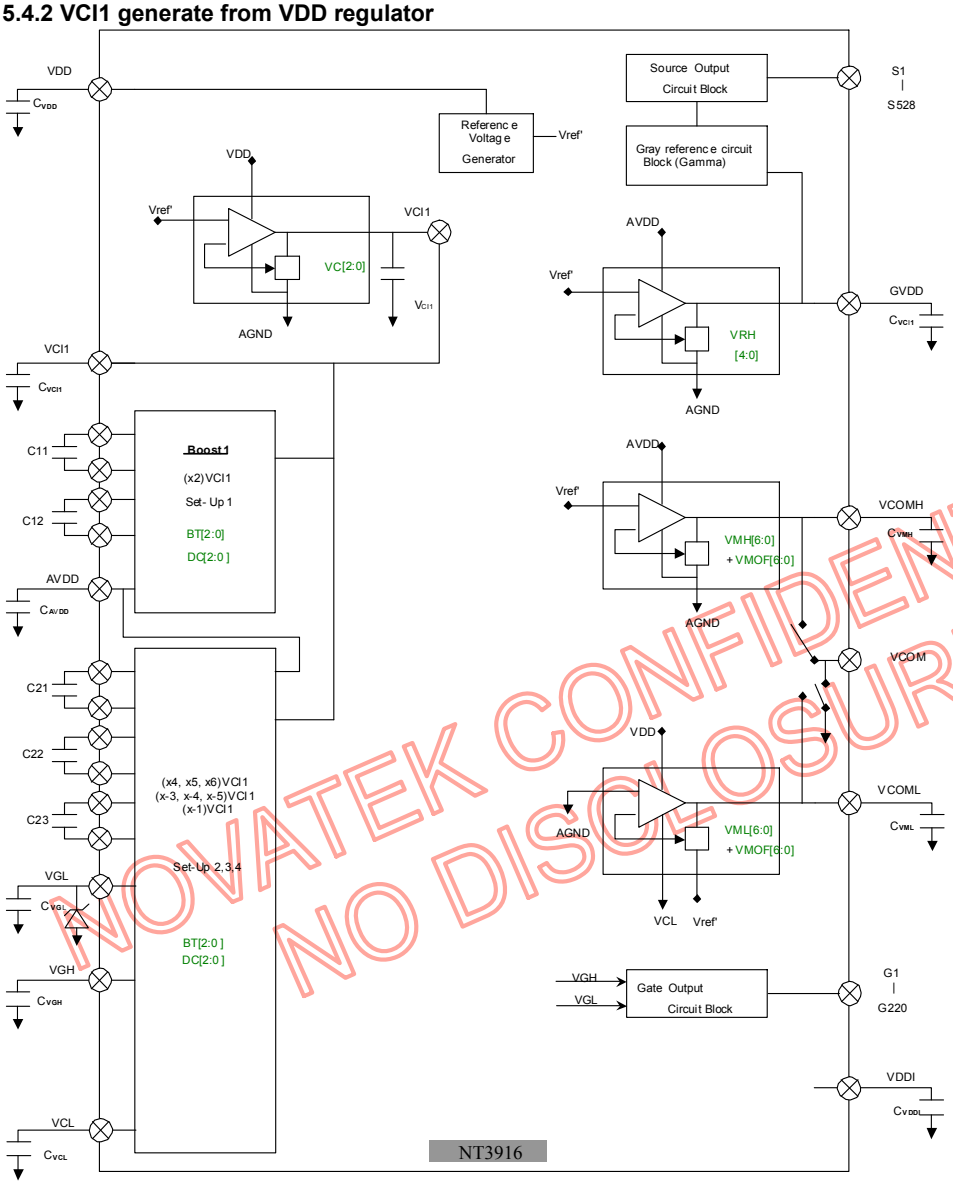


Fig 5.4.2 Power Booster Structure (1)

5.4.3 VCI1 = VDD

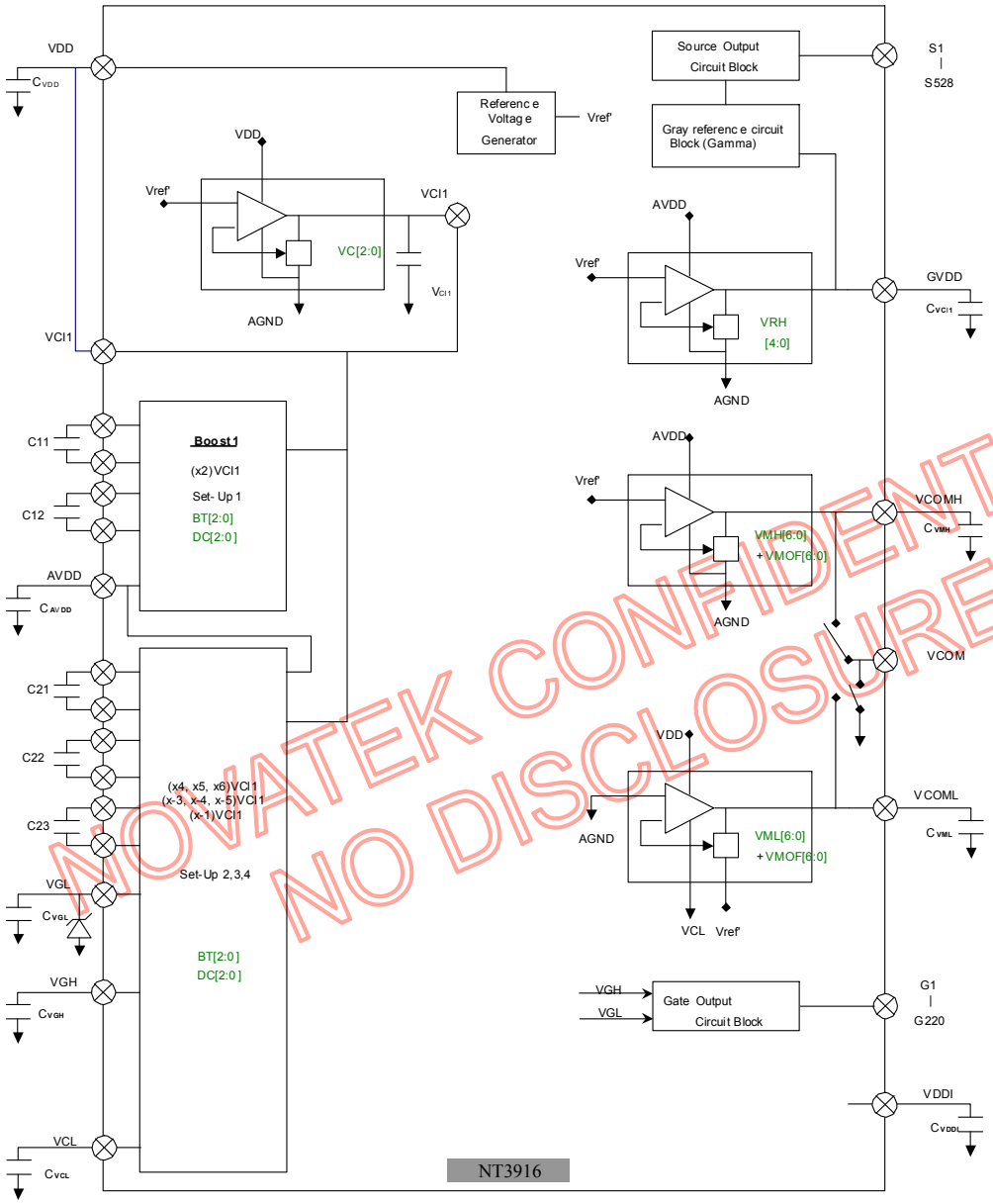


Fig 5.4.3 Power Booster Structure (2) VCI1=VDD

Note: In this case, external power VDD ≤ VCI1 setting value.

5.4.4 EXTERNAL COMPONENTS CONNECTION

Pad Name	Connection	Rated (Min)Voltage	Typical capacitance value
VDDI	VDDI (Logic Power)		
VDD	VDD (Analog Power)		
VCC	Connect to Capacitor (Max 2V): VCC -------||-------- GND	5.0V	1.0 uF
VCI1	Connect to Capacitor (Max 2.75V): VCI1 -------||----- GND	5.0V	1.0 uF
AGND	Analog ground (Connect to GND)		
DGND	Digital ground (Connect to GND)		
C23P, C23N	Connect to Capacitor: C23P -------||--------C23N	6.0V	1.0 uF
C22P, C22N	Connect to Capacitor: C22P -------||--------C22N	6.0V	1.0 uF
C21P, C22N	Connect to Capacitor: C21P -------||--------C21N	6.0V	1.0 uF
C12P, C12N	Connect to Capacitor: C12P -------||--------C12N	6.0V	1.0 uF
C11P, C11N	Connect to Capacitor: C11P -------||--------C11N	6.0V	1.0 uF
AVDD	Connect to Capacitor: AVDD -------||-------- GND	6.0V	2.2 uF
VGH	Connect to Capacitor: VGH -------||-------- GND	18.0V	0.1 uF
VGL	Connect to Capacitor: VGL -------||-------- GND	16.0V	0.1 uF
VCL	Connect to Capacitor: VCL -------||-------- GND	5.0V	1.0 uF
VREF	Connect to Capacitor: VREF -------||-------- GND	6.0V	1.0 uF
GVDD	Connect to Capacitor: GVDD -------||-------- GND	6.0V	1.0 uF
VCOMH	Connect to Capacitor: VCOMH-------||--------- GND	6.0V	1.0 uF
VCOML	Connect to Capacitor: VCOML -------||-------- GND	5.0V	1.0 uF
VGL	Connect to Schottky diode: VGL -------►|-------- GND	30V	Schottky diode **VF<=0.4V at 20mA VR >=30V**

5.5 Gamma structure

5.5.1 Relationship between RAM Data and Output Voltages for ECB-type LCD default setting.

Data	Output Voltage (LCM=11, ECB-type)									
(Hex)	VCOM = Low					VCOM = High				
	Gamma	2.2				Gamma	2.2			
		R	G	B	Gray		R	G	B	Gray
0	V0+	4.550	4.550	4.550	4.550	V0-	0.276	0.313	0.282	0.315
1	V1+	4.453	4.458	4.550	4.424	V1-	0.379	0.382	0.317	0.455
2	V2+	4.340	4.346	4.441	4.318	V2-	0.495	0.494	0.421	0.558
3	V3+	4.219	4.226	4.324	4.203	V3-	0.619	0.614	0.532	0.668
4	V4+	4.089	4.097	4.198	4.081	V4-	0.753	0.743	0.652	0.787
5	V5+	3.967	3.976	4.080	3.967	V5-	0.877	0.863	0.763	0.898
6	V6+	3.855	3.865	3.971	3.861	V6-	0.993	0.975	0.867	1.000
7	V7+	3.751	3.762	3.871	3.763	V7-	1.100	1.078	0.963	1.095
8	V8+	3.646	3.658	3.770	3.665	V8-	1.206	1.181	1.058	1.190
9	V9+	3.555	3.567	3.678	3.572	V9-	1.296	1.271	1.150	1.285
0A	V10+	3.463	3.476	3.587	3.478	V10-	1.386	1.361	1.241	1.380
0B	V11+	3.380	3.394	3.503	3.393	V11-	1.467	1.444	1.325	1.467
0C	V12+	3.305	3.319	3.428	3.316	V12-	1.540	1.517	1.400	1.545
0D	V13+	3.238	3.253	3.362	3.248	V13-	1.605	1.583	1.466	1.614
0E	V14+	3.180	3.195	3.303	3.189	V14-	1.663	1.640	1.525	1.675
0F	V15+	3.121	3.137	3.245	3.129	V15-	1.720	1.698	1.583	1.735
10	V16+	3.071	3.087	3.195	3.078	V16-	1.768	1.747	1.633	1.787
11	V17+	3.021	3.038	3.145	3.027	V17-	1.817	1.796	1.683	1.839
12	V18+	2.971	2.988	3.095	2.976	V18-	1.866	1.846	1.733	1.891
13	V19+	2.930	2.947	3.053	2.934	V19-	1.907	1.887	1.775	1.934
14	V20+	2.888	2.905	3.012	2.891	V20-	1.948	1.928	1.816	1.978
15	V21+	2.853	2.869	2.974	2.852	V21-	1.985	1.963	1.855	2.015
16	V22+	2.818	2.832	2.936	2.813	V22-	2.022	1.999	1.893	2.053
17	V23+	2.783	2.796	2.898	2.774	V23-	2.059	2.035	1.931	2.091
18	V24+	2.748	2.759	2.860	2.735	V24-	2.097	2.071	1.969	2.129
19	V25+	2.713	2.723	2.822	2.696	V25-	2.134	2.107	2.007	2.167
1A	V26+	2.686	2.694	2.791	2.668	V26-	2.164	2.135	2.038	2.197
1B	V27+	2.658	2.665	2.761	2.633	V27-	2.194	2.164	2.068	2.228
1C	V28+	2.630	2.636	2.731	2.602	V28-	2.224	2.193	2.099	2.258
1D	V29+	2.602	2.606	2.700	2.571	V29-	2.254	2.221	2.130	2.288
1E	V30+	2.574	2.577	2.670	2.539	V30-	2.283	2.250	2.160	2.318
1F	V31+	2.546	2.548	2.640	2.508	V31-	2.313	2.279	2.191	2.349
20	V32+	2.518	2.519	2.609	2.477	V32-	2.343	2.307	2.221	2.379
21	V33+	2.490	2.490	2.579	2.446	V33-	2.373	2.336	2.252	2.409
22	V34+	2.462	2.461	2.548	2.414	V34-	2.403	2.365	2.282	2.440
23	V35+	2.434	2.431	2.518	2.383	V35-	2.433	2.393	2.313	2.470
24	V36+	2.406	2.402	2.488	2.352	V36-	2.462	2.422	2.343	2.500
25	V37+	2.378	2.373	2.457	2.320	V37-	2.492	2.450	2.374	2.531
26	V38+	2.350	2.344	2.427	2.289	V38-	2.522	2.479	2.404	2.561
27	V39+	2.322	2.315	2.397	2.258	V39-	2.552	2.508	2.435	2.591
28	V40+	2.294	2.286	2.366	2.227	V40-	2.582	2.536	2.466	2.622
29	V41+	2.266	2.256	2.336	2.195	V41-	2.612	2.565	2.496	2.652
2A	V42+	2.238	2.227	2.305	2.164	V42-	2.642	2.594	2.527	2.682
2B	V43+	2.210	2.198	2.275	2.133	V43-	2.671	2.622	2.557	2.713
2C	V44+	2.174	2.169	2.244	2.105	V44-	2.704	2.653	2.588	2.743
2D	V45+	2.138	2.139	2.213	2.077	V45-	2.738	2.683	2.619	2.774
2E	V46+	2.102	2.110	2.181	2.049	V46-	2.771	2.714	2.650	2.805
2F	V47+	2.066	2.080	2.150	2.022	V47-	2.804	2.745	2.681	2.836
30	V48+	2.030	2.051	2.119	1.994	V48-	2.837	2.775	2.712	2.867
31	V49+	1.994	2.021	2.088	1.966	V49-	2.870	2.806	2.743	2.897
32	V50+	1.957	1.992	2.057	1.938	V50-	2.903	2.836	2.774	2.928
33	V51+	1.921	1.962	2.025	1.910	V51-	2.936	2.867	2.805	2.959
34	V52+	1.885	1.933	1.994	1.883	V52-	2.969	2.897	2.837	2.990
35	V53+	1.849	1.903	1.963	1.855	V53-	3.002	2.928	2.868	3.021
36	V54+	1.804	1.866	1.924	1.820	V54-	3.044	2.966	2.906	3.059
37	V55+	1.759	1.829	1.885	1.785	V55-	3.085	3.004	2.945	3.098
38	V56+	1.705	1.775	1.837	1.733	V56-	3.138	3.060	2.995	3.150
39	V57+	1.652	1.722	1.790	1.681	V57-	3.192	3.116	3.044	3.203
3A	V58+	1.588	1.657	1.732	1.618	V58-	3.256	3.182	3.103	3.266
3B	V59+	1.514	1.582	1.666	1.545	V59-	3.331	3.260	3.172	3.339
3C	V60+	1.429	1.496	1.589	1.462	V60-	3.416	3.349	3.251	3.423
3D	V61+	1.333	1.399	1.504	1.368	V61-	3.512	3.449	3.340	3.518
3E	V62+	1.226	1.291	1.408	1.264	V62-	3.619	3.560	3.439	3.623
3F	V63+	0.581	0.584	0.823	0.569	V63-	4.274	4.272	4.021	4.305

Data	Output Voltage (LCM=11, ECB-type)							
(Hex)	VCOM = Low				VCOM = High			
	Gamma	1	1.8	2.5	Gamma	1	1.8	2.5
0	V0+	4.550	4.550	4.550	V0-	0.286	0.301	0.322
1	V1+	3.502	4.288	4.550	V1-	1.316	0.602	0.322
2	V2+	3.394	4.160	4.452	V2-	1.432	0.728	0.418
3	V3+	3.276	4.022	4.346	V3-	1.557	0.864	0.522
4	V4+	3.151	3.874	4.232	V4-	1.691	1.009	0.633
5	V5+	3.034	3.736	4.126	V5-	1.816	1.145	0.737
6	V6+	2.925	3.608	4.028	V6-	1.932	1.271	0.833
7	V7+	2.824	3.490	3.937	V7-	2.039	1.388	0.922
8	V8+	2.724	3.372	3.846	V8-	2.146	1.504	1.011
9	V9+	2.672	3.290	3.741	V9-	2.196	1.584	1.114
0A	V10+	2.619	3.209	3.637	V10-	2.247	1.663	1.217
0B	V11+	2.571	3.136	3.541	V11-	2.292	1.736	1.310
0C	V12+	2.528	3.069	3.455	V12-	2.333	1.801	1.394
0D	V13+	2.490	3.010	3.379	V13-	2.370	1.858	1.469
0E	V14+	2.457	2.959	3.312	V14-	2.402	1.909	1.534
0F	V15+	2.424	2.907	3.246	V15-	2.433	1.960	1.600
10	V16+	2.395	2.863	3.188	V16-	2.461	2.003	1.656
11	V17+	2.366	2.819	3.131	V17-	2.488	2.046	1.712
12	V18+	2.338	2.774	3.074	V18-	2.516	2.090	1.768
13	V19+	2.314	2.737	3.026	V19-	2.538	2.126	1.815
14	V20+	2.290	2.701	2.979	V20-	2.561	2.162	1.861
15	V21+	2.267	2.667	2.940	V21-	2.585	2.195	1.902
16	V22+	2.244	2.633	2.901	V22-	2.608	2.228	1.942
17	V23+	2.221	2.599	2.863	V23-	2.632	2.261	1.982
18	V24+	2.197	2.566	2.824	V24-	2.656	2.294	2.022
19	V25+	2.174	2.532	2.785	V25-	2.679	2.327	2.063
1A	V26+	2.156	2.505	2.754	V26-	2.698	2.353	2.095
1B	V27+	2.137	2.478	2.723	V27-	2.717	2.380	2.127
1C	V28+	2.119	2.451	2.692	V28-	2.736	2.406	2.159
1D	V29+	2.100	2.424	2.661	V29-	2.755	2.432	2.192
1E	V30+	2.082	2.397	2.630	V30-	2.774	2.459	2.224
1F	V31+	2.063	2.370	2.599	V31-	2.792	2.485	2.256
20	V32+	2.045	2.343	2.569	V32-	2.811	2.511	2.288
21	V33+	2.026	2.316	2.538	V33-	2.830	2.538	2.320
22	V34+	2.008	2.289	2.507	V34-	2.849	2.564	2.353
23	V35+	1.989	2.262	2.476	V35-	2.868	2.591	2.385
24	V36+	1.971	2.235	2.445	V36-	2.887	2.617	2.417
25	V37+	1.952	2.208	2.414	V37-	2.906	2.643	2.449
26	V38+	1.934	2.181	2.383	V38-	2.925	2.670	2.482
27	V39+	1.915	2.154	2.352	V39-	2.944	2.696	2.514
28	V40+	1.897	2.127	2.321	V40-	2.962	2.722	2.546
29	V41+	1.878	2.100	2.290	V41-	2.981	2.749	2.578
2A	V42+	1.859	2.073	2.259	V42-	3.000	2.775	2.610
2B	V43+	1.841	2.046	2.228	V43-	3.019	2.801	2.643
2C	V44+	1.816	2.017	2.192	V44-	3.042	2.830	2.676
2D	V45+	1.791	1.988	2.157	V45-	3.065	2.859	2.709
2E	V46+	1.766	1.959	2.121	V46-	3.088	2.887	2.742
2F	V47+	1.740	1.931	2.085	V47-	3.111	2.916	2.775
30	V48+	1.715	1.902	2.050	V48-	3.133	2.944	2.808
31	V49+	1.690	1.873	2.014	V49-	3.156	2.973	2.841
32	V50+	1.665	1.844	1.979	V50-	3.179	3.001	2.874
33	V51+	1.640	1.815	1.943	V51-	3.202	3.030	2.907
34	V52+	1.615	1.787	1.907	V52-	3.225	3.059	2.940
35	V53+	1.590	1.758	1.872	V53-	3.248	3.087	2.974
36	V54+	1.558	1.722	1.827	V54-	3.277	3.123	3.015
37	V55+	1.527	1.686	1.782	V55-	3.305	3.159	3.056
38	V56+	1.483	1.638	1.731	V56-	3.352	3.208	3.111
39	V57+	1.440	1.591	1.679	V57-	3.400	3.256	3.167
3A	V58+	1.388	1.534	1.617	V58-	3.456	3.315	3.233
3B	V59+	1.327	1.467	1.545	V59-	3.522	3.384	3.310
3C	V60+	1.258	1.392	1.463	V60-	3.598	3.462	3.398
3D	V61+	1.179	1.306	1.370	V61-	3.683	3.550	3.498
3E	V62+	1.093	1.211	1.266	V62-	3.777	3.648	3.608
3F	V63+	0.569	0.589	0.563	V63-	4.264	4.287	4.274

5.5.2 Relationship between RAM Data and Output Voltages for TM-type LCD default setting.

Data	Output Voltage (LCM=11, ECB-type)									
(Hex)	VCOM = Low					VCOM = High				
	Gamma	2.2				Gamma	2.2			
		R	G	B	Gray		R	G	B	Gray
0	V0+	4.550	4.550	4.464	4.550	V0-	0.127	0.126	0.135	0.253
1	V1+	4.550	4.550	4.464	4.478	V1-	0.191	0.188	0.135	0.397
2	V2+	4.425	4.425	4.362	4.377	V2-	0.333	0.329	0.271	0.498
3	V3+	4.290	4.290	4.252	4.268	V3-	0.487	0.480	0.419	0.607
4	V4+	4.145	4.145	4.135	4.152	V4-	0.651	0.642	0.576	0.723
5	V5+	4.010	4.010	4.025	4.043	V5-	0.804	0.793	0.723	0.832
6	V6+	3.885	3.885	3.923	3.942	V6-	0.946	0.933	0.860	0.933
7	V7+	3.769	3.769	3.829	3.849	V7-	1.078	1.063	0.986	1.026
8	V8+	3.654	3.654	3.734	3.756	V8-	1.209	1.192	1.112	1.119
9	V9+	3.556	3.560	3.638	3.649	V9-	1.299	1.282	1.204	1.226
0A	V10+	3.458	3.466	3.542	3.542	V10-	1.390	1.371	1.296	1.333
0B	V11+	3.369	3.381	3.455	3.444	V11-	1.472	1.452	1.379	1.431
0C	V12+	3.289	3.304	3.377	3.357	V12-	1.546	1.525	1.454	1.518
0D	V13+	3.218	3.236	3.307	3.279	V13-	1.612	1.589	1.521	1.596
0E	V14+	3.155	3.177	3.246	3.211	V14-	1.669	1.646	1.579	1.664
0F	V15+	3.093	3.117	3.185	3.143	V15-	1.727	1.703	1.637	1.732
10	V16+	3.040	3.066	3.132	3.085	V16-	1.776	1.752	1.687	1.790
11	V17+	2.986	3.015	3.080	3.026	V17-	1.825	1.800	1.737	1.849
12	V18+	2.933	2.963	3.028	2.968	V18-	1.875	1.849	1.787	1.907
13	V19+	2.888	2.921	2.984	2.919	V19-	1.916	1.889	1.829	1.956
14	V20+	2.844	2.878	2.940	2.871	V20-	1.957	1.930	1.871	2.004
15	V21+	2.815	2.850	2.912	2.834	V21-	1.988	1.961	1.902	2.038
16	V22+	2.787	2.821	2.883	2.796	V22-	2.019	1.991	1.933	2.071
17	V23+	2.758	2.793	2.854	2.759	V23-	2.050	2.022	1.964	2.105
18	V24+	2.730	2.765	2.825	2.722	V24-	2.081	2.053	1.996	2.138
19	V25+	2.702	2.736	2.797	2.685	V25-	2.113	2.083	2.027	2.172
1A	V26+	2.679	2.713	2.773	2.655	V26-	2.138	2.108	2.052	2.198
1B	V27+	2.656	2.691	2.750	2.625	V27-	2.162	2.133	2.077	2.225
1C	V28+	2.633	2.668	2.727	2.595	V28-	2.187	2.157	2.102	2.252
1D	V29+	2.611	2.645	2.704	2.566	V29-	2.212	2.182	2.127	2.279
1E	V30+	2.588	2.622	2.681	2.536	V30-	2.237	2.206	2.152	2.306
1F	V31+	2.565	2.600	2.658	2.506	V31-	2.262	2.231	2.177	2.333
20	V32+	2.542	2.577	2.635	2.476	V32-	2.287	2.256	2.202	2.359
21	V33+	2.520	2.554	2.612	2.446	V33-	2.312	2.280	2.227	2.386
22	V34+	2.497	2.531	2.589	2.417	V34-	2.337	2.305	2.252	2.413
23	V35+	2.474	2.509	2.566	2.387	V35-	2.362	2.329	2.277	2.440
24	V36+	2.451	2.486	2.543	2.357	V36-	2.387	2.354	2.302	2.467
25	V37+	2.429	2.463	2.520	2.327	V37-	2.412	2.379	2.327	2.493
26	V38+	2.406	2.440	2.497	2.298	V38-	2.437	2.403	2.352	2.520
27	V39+	2.383	2.418	2.474	2.268	V39-	2.462	2.428	2.377	2.547
28	V40+	2.360	2.395	2.451	2.238	V40-	2.487	2.452	2.402	2.574
29	V41+	2.338	2.372	2.428	2.208	V41-	2.512	2.477	2.427	2.601
2A	V42+	2.315	2.349	2.405	2.178	V42-	2.536	2.501	2.452	2.627
2B	V43+	2.292	2.327	2.382	2.149	V43-	2.561	2.526	2.477	2.654
2C	V44+	2.266	2.301	2.357	2.123	V44-	2.588	2.552	2.500	2.683
2D	V45+	2.240	2.274	2.331	2.097	V45-	2.615	2.579	2.523	2.712
2E	V46+	2.214	2.248	2.305	2.071	V46-	2.642	2.605	2.546	2.741
2F	V47+	2.187	2.222	2.279	2.045	V47-	2.668	2.631	2.569	2.770
30	V48+	2.161	2.196	2.254	2.019	V48-	2.695	2.658	2.592	2.799
31	V49+	2.135	2.170	2.228	1.993	V49-	2.722	2.684	2.615	2.828
32	V50+	2.109	2.143	2.202	1.967	V50-	2.748	2.711	2.638	2.856
33	V51+	2.083	2.117	2.176	1.941	V51-	2.775	2.737	2.661	2.885
34	V52+	2.056	2.091	2.151	1.915	V52-	2.802	2.763	2.683	2.914
35	V53+	2.030	2.065	2.125	1.889	V53-	2.829	2.790	2.706	2.943
36	V54+	1.998	2.032	2.093	1.856	V54-	2.862	2.823	2.735	2.979
37	V55+	1.965	1.999	2.060	1.824	V55-	2.895	2.856	2.764	3.015
38	V56+	1.930	1.961	2.026	1.782	V56-	2.930	2.895	2.801	3.059
39	V57+	1.896	1.923	1.992	1.741	V57-	2.965	2.934	2.838	3.102
3A	V58+	1.854	1.878	1.950	1.691	V58-	3.007	2.981	2.882	3.154
3B	V59+	1.806	1.825	1.902	1.633	V59-	3.056	3.036	2.934	3.215
3C	V60+	1.751	1.764	1.847	1.566	V60-	3.112	3.099	2.994	3.284
3D	V61+	1.689	1.696	1.786	1.491	V61-	3.175	3.169	3.060	3.362
3E	V62+	1.620	1.620	1.717	1.408	V62-	3.245	3.248	3.134	3.449
3F	V63+	0.586	0.586	0.601	0.686	V63-	4.264	4.268	4.247	4.153

Data	Output Voltage (LCM=01, TM-type)							
(Hex)	VCOM = Low				VCOM = High			
	Gamma	1	1.8	2.5	Gamma	1	1.8	2.5
0	V0+	4.495	4.495	4.495	V0-	0.355	0.355	0.355
1	V1+	3.515	4.350	4.451	V1-	1.335	0.500	0.399
2	V2+	3.283	4.135	4.407	V2-	1.567	0.715	0.443
3	V3+	3.150	3.939	4.364	V3-	1.700	0.911	0.486
4	V4+	3.056	3.785	4.262	V4-	1.794	1.065	0.588
5	V5+	2.980	3.651	4.156	V5-	1.870	1.199	0.694
6	V6+	2.918	3.544	4.049	V6-	1.932	1.306	0.801
7	V7+	2.865	3.450	3.942	V7-	1.985	1.400	0.908
8	V8+	2.816	3.367	3.845	V8-	2.034	1.483	1.005
9	V9+	2.780	3.300	3.751	V9-	2.070	1.550	1.099
0A	V10+	2.737	3.237	3.664	V10-	2.113	1.613	1.186
0B	V11+	2.705	3.177	3.586	V11-	2.145	1.673	1.264
0C	V12+	2.668	3.134	3.515	V12-	2.182	1.716	1.335
0D	V13+	2.639	3.086	3.447	V13-	2.211	1.764	1.403
0E	V14+	2.604	3.042	3.382	V14-	2.246	1.808	1.468
0F	V15+	2.579	2.997	3.322	V15-	2.271	1.853	1.528
10	V16+	2.556	2.956	3.275	V16-	2.294	1.894	1.575
11	V17+	2.519	2.920	3.225	V17-	2.331	1.930	1.625
12	V18+	2.499	2.883	3.174	V18-	2.351	1.967	1.676
13	V19+	2.479	2.851	3.137	V19-	2.371	1.999	1.713
14	V20+	2.455	2.817	3.096	V20-	2.395	2.033	1.754
15	V21+	2.431	2.789	3.053	V21-	2.419	2.061	1.797
16	V22+	2.418	2.757	3.015	V22-	2.432	2.093	1.835
17	V23+	2.395	2.728	2.975	V23-	2.455	2.122	1.875
18	V24+	2.373	2.702	2.937	V24-	2.477	2.148	1.913
19	V25+	2.357	2.671	2.903	V25-	2.493	2.179	1.947
1A	V26+	2.335	2.644	2.870	V26-	2.515	2.206	1.980
1B	V27+	2.314	2.615	2.837	V27-	2.536	2.235	2.013
1C	V28+	2.298	2.588	2.802	V28-	2.552	2.262	2.048
1D	V29+	2.282	2.565	2.778	V29-	2.568	2.285	2.072
1E	V30+	2.266	2.537	2.741	V30-	2.584	2.313	2.109
1F	V31+	2.243	2.508	2.714	V31-	2.607	2.342	2.136
20	V32+	2.223	2.487	2.685	V32-	2.627	2.363	2.165
21	V33+	2.205	2.464	2.652	V33-	2.645	2.386	2.198
22	V34+	2.187	2.434	2.623	V34-	2.663	2.416	2.227
23	V35+	2.169	2.420	2.591	V35-	2.681	2.430	2.259
24	V36+	2.153	2.395	2.566	V36-	2.697	2.455	2.284
25	V37+	2.134	2.371	2.533	V37-	2.716	2.479	2.317
26	V38+	2.112	2.350	2.503	V38-	2.738	2.500	2.347
27	V39+	2.095	2.322	2.479	V39-	2.755	2.528	2.371
28	V40+	2.078	2.301	2.448	V40-	2.772	2.549	2.402
29	V41+	2.058	2.281	2.424	V41-	2.792	2.569	2.426
2A	V42+	2.041	2.257	2.399	V42-	2.809	2.593	2.451
2B	V43+	2.024	2.229	2.369	V43-	2.826	2.621	2.481
2C	V44+	2.001	2.205	2.342	V44-	2.849	2.645	2.508
2D	V45+	1.980	2.180	2.311	V45-	2.870	2.670	2.539
2E	V46+	1.960	2.157	2.287	V46-	2.890	2.693	2.563
2F	V47+	1.944	2.130	2.259	V47-	2.906	2.720	2.591
30	V48+	1.929	2.102	2.224	V48-	2.921	2.748	2.626
31	V49+	1.913	2.076	2.194	V49-	2.937	2.774	2.656
32	V50+	1.896	2.048	2.163	V50-	2.954	2.802	2.687
33	V51+	1.880	2.023	2.130	V51-	2.970	2.827	2.720
34	V52+	1.864	1.988	2.095	V52-	2.986	2.862	2.755
35	V53+	1.847	1.957	2.060	V53-	3.003	2.893	2.790
36	V54+	1.829	1.933	2.027	V54-	3.021	2.917	2.823
37	V55+	1.808	1.908	1.982	V55-	3.042	2.942	2.868
38	V56+	1.783	1.880	1.945	V56-	3.067	2.970	2.905
39	V57+	1.757	1.854	1.912	V57-	3.093	2.996	2.938
3A	V58+	1.730	1.823	1.876	V58-	3.120	3.027	2.974
3B	V59+	1.698	1.784	1.840	V59-	3.152	3.066	3.010
3C	V60+	1.659	1.738	1.790	V60-	3.191	3.112	3.060
3D	V61+	1.596	1.681	1.727	V61-	3.254	3.169	3.123
3E	V62+	1.526	1.581	1.629	V62-	3.324	3.269	3.221
3F	V63+	0.785	0.785	0.785	V63-	4.065	4.065	4.065

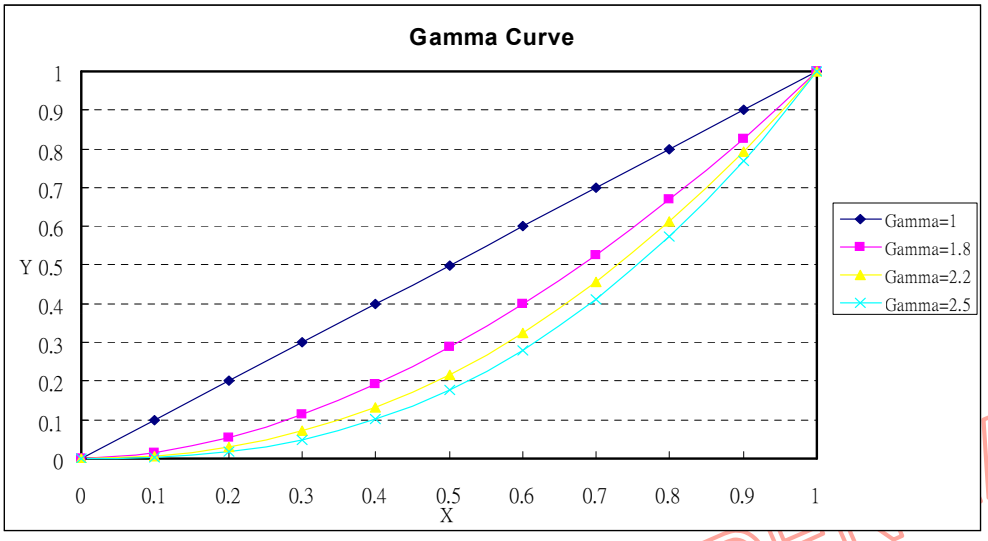


Fig. 5.5.2.1 Gamma Curve according to the GC0 to GC3 bit

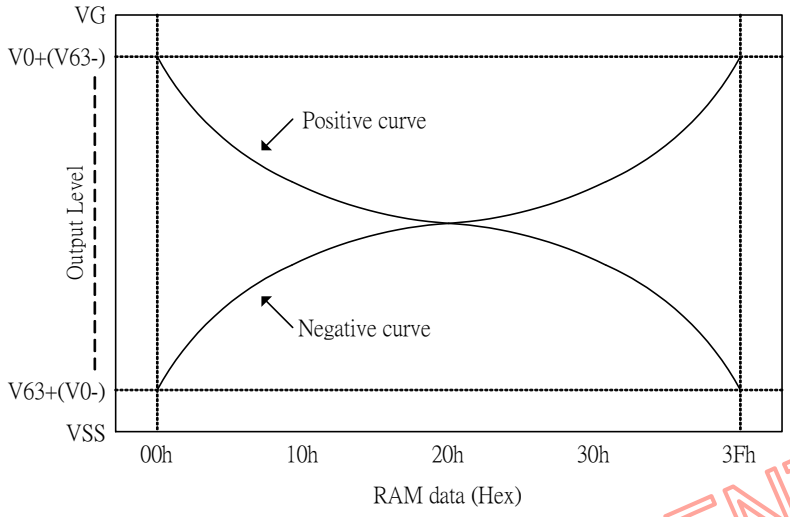


Fig. 5.5.2.2 Relationship between RAM data and output level

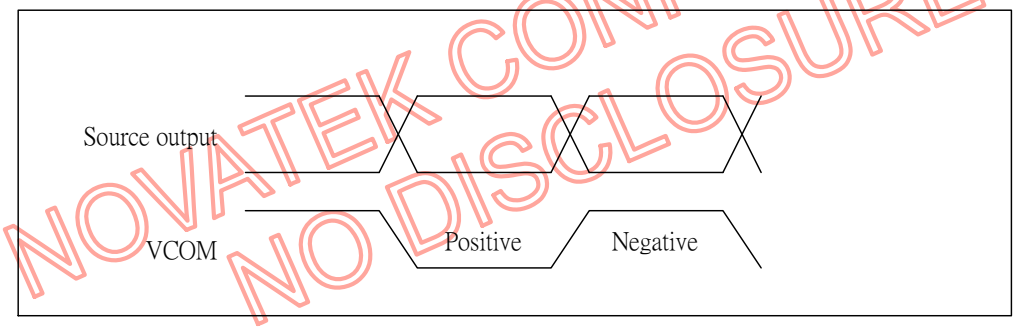


Fig. 5.5.2.3 Relationship between source output and VCOM

5.6 Power ON/OFF Sequence

VDDI and VDD can be applied in any order.
VDDI and VDD can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.
During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

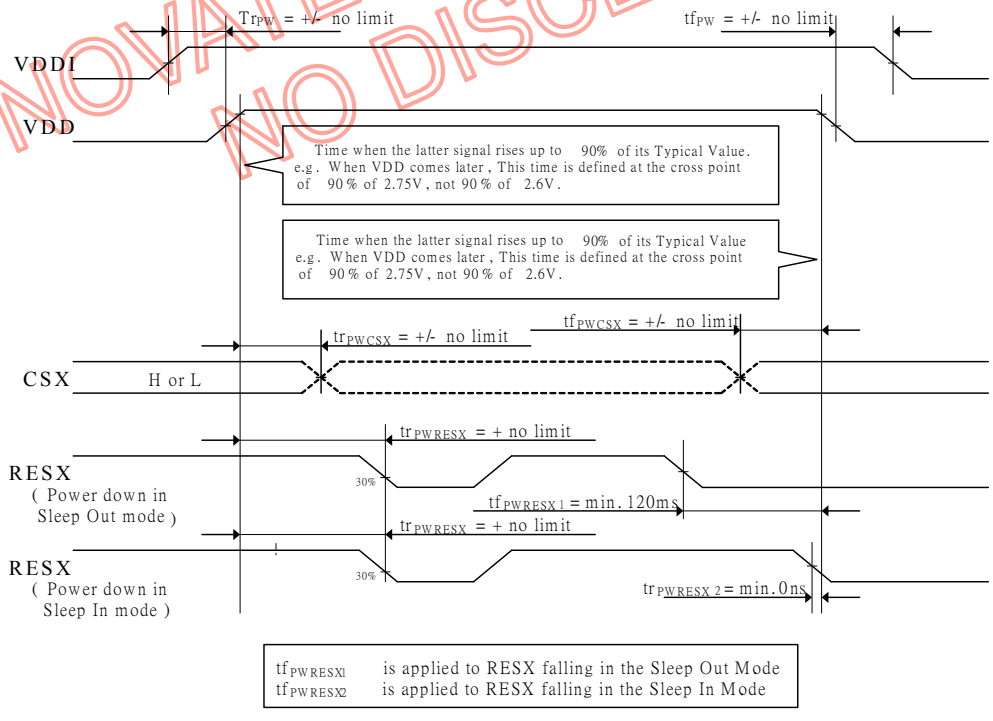
Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

If RESX line is not held stable by host during Power On Sequence as defined in Sections 8.5.1 and 8.5.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below:

5.6.1 Case 1 – RESX Line is held High or Unstable by Host at Power On

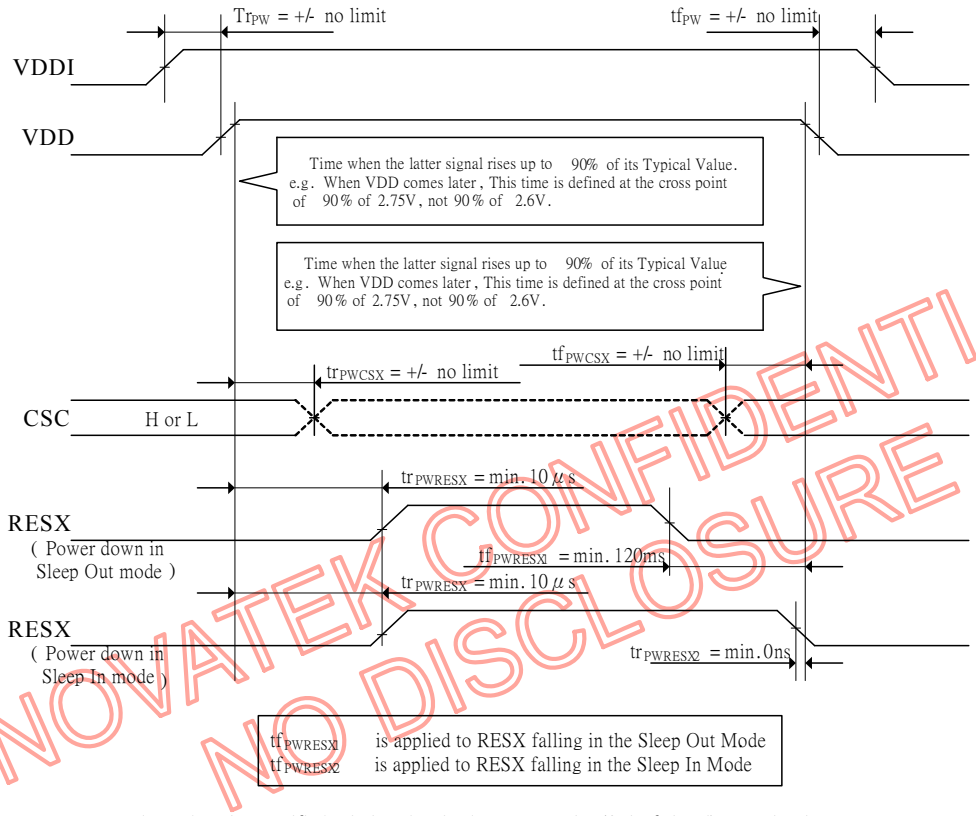
If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDD and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Note: Unless otherwise specified, timings herein show cross point at 50 % of signal/power level

5.6.2 Case 2 – RESX Line is Held Low by Host at Power On

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VDD and VDDI have been applied.



Note: Unless otherwise specified timings herein show cross point at 50 % of signal power level

5.6.3 Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface.

2. At an uncontrolled power off the display will go blank and there will not be any visible effects within (TBD) second on the display (blank display) and remains blank until "Power On Sequence" powers it up.

5.7 Power Level Definition

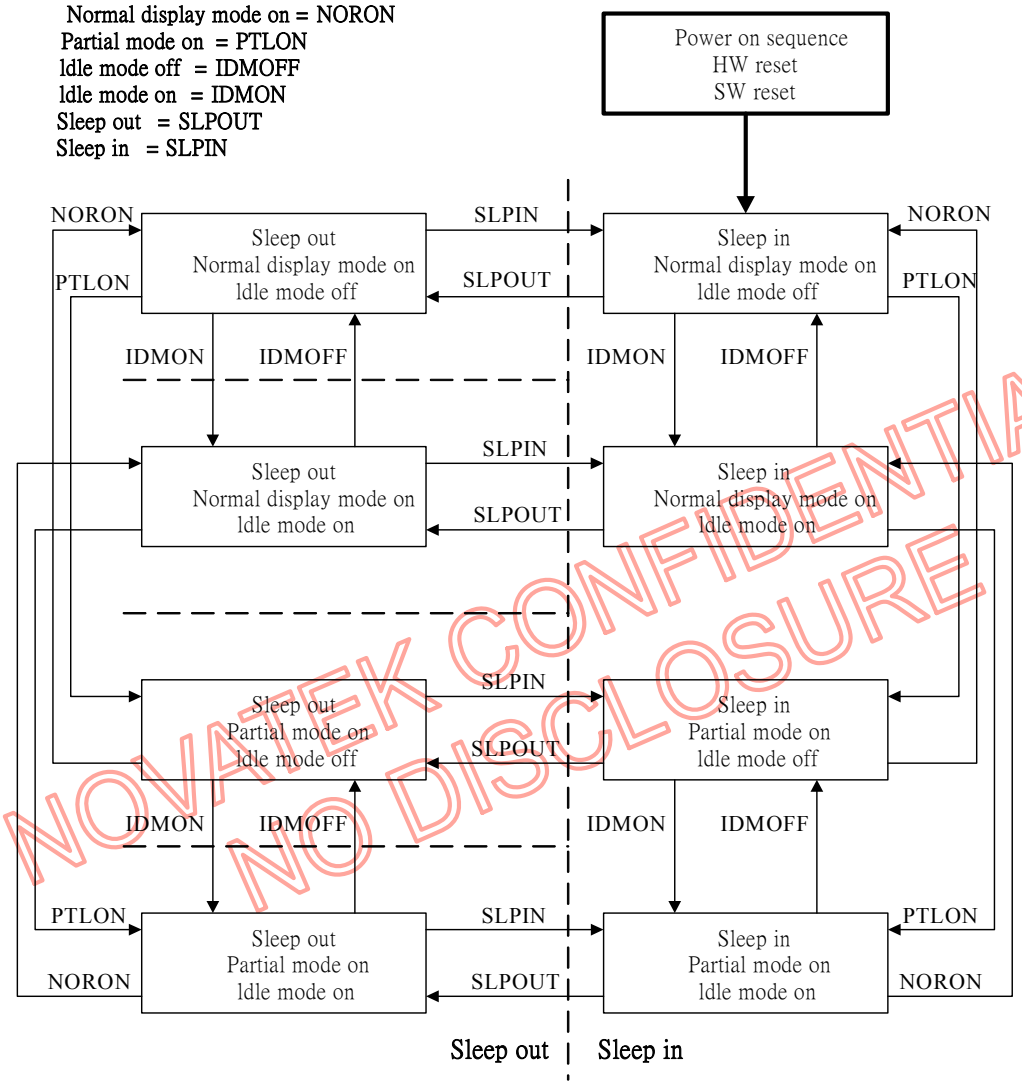
5.7.1 Power Level

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. **Normal Mode On (full display), Idle Mode Off, Sleep Out.**
   In this mode, the display is able to show maximum 262,144 colors.
2. **Partial Mode On, Idle Mode Off, Sleep Out.**
   In this mode part of the display is used with maximum 262,144 colors.
3. **Normal Mode On (full display), Idle Mode On, Sleep Out.**
   In this mode, the full display area is used but with 8 colors.
4. **Partial Mode On, Idle Mode On, Sleep Out.**
   In this mode, part of the display is used but with 8 colors.
5. **Sleep In Mode**
   In this mode, the DC: DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU Interface and memory works with VDDI power supply. Contents of the memory are safe.
6. **Power Off Mode**
   In this mode, both VDD and VDDI are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

5.7.2 Power Flow Chart



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by this spec, when there is changing from one power mode to another power mode.

5.8 INPUT / OUTPUT PIN STATE

5.8.1 Output or Bi-directional (I/O) Pins

Output or Bi-directional pins	After Power On	After Hardware Reset	After Software Reset
TE	Low	Low	Low
D7 to D0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)

Note: There will be no output from D7-D0 during Power On/Off sequence, Hardware Reset and Software Reset.

5.8.2 Input Pins

Input pins	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
RESX	See 5.6	Input valid	Input valid	Input valid	See 5.6
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input valid	Input Invalid
D17 to D0	Input invalid	Input valid	Input valid	Input valid	input invalid
SPI_CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
SCL	Input invalid	Input valid	Input valid	Input valid	Input invalid
SDA	Input invalid	Input valid	Input valid	Input valid	input invalid

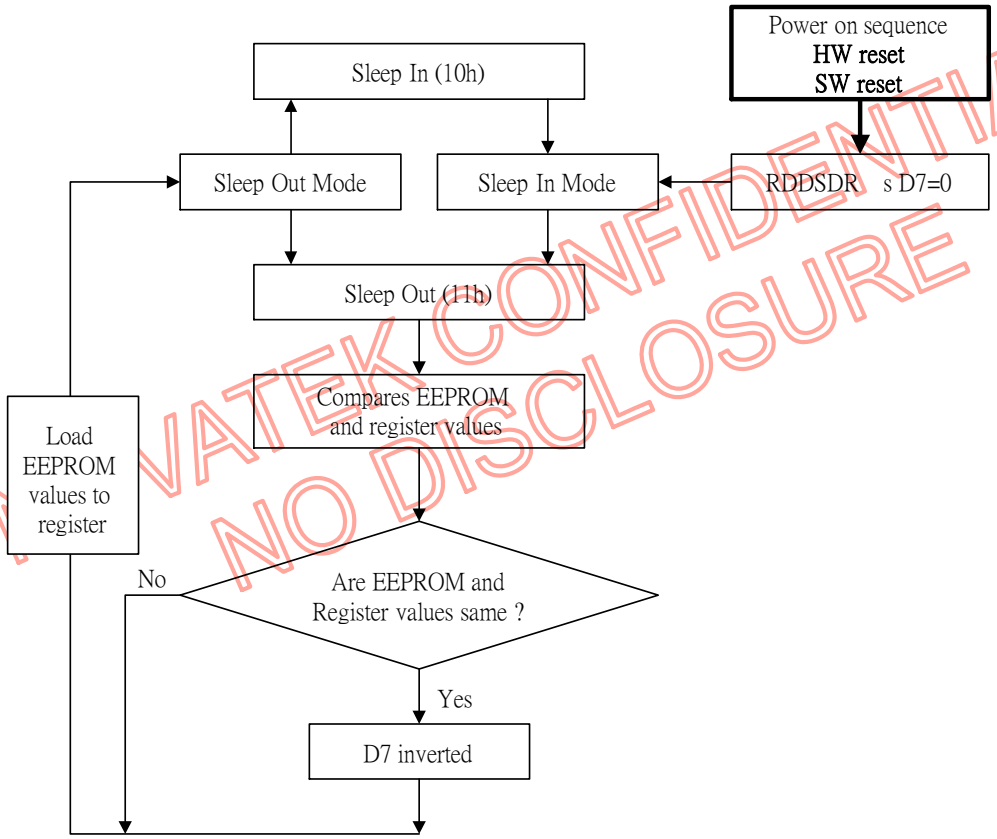
5.9 Sleep Out-Command and Self-Diagnostic Functions of the Display Module

5.9.1 Register Loading Detection

Sleep Out-command (See section 6.1.12 "Sleep Out (11h)") is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the EEPROM and register values of the display controller by the display controller. If those both values (EEPROM and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command 6.1.10 "Read Display Self-Diagnostic Result (0Fh)" (=RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= increased by 1).

The flow chart for this internal function is following:



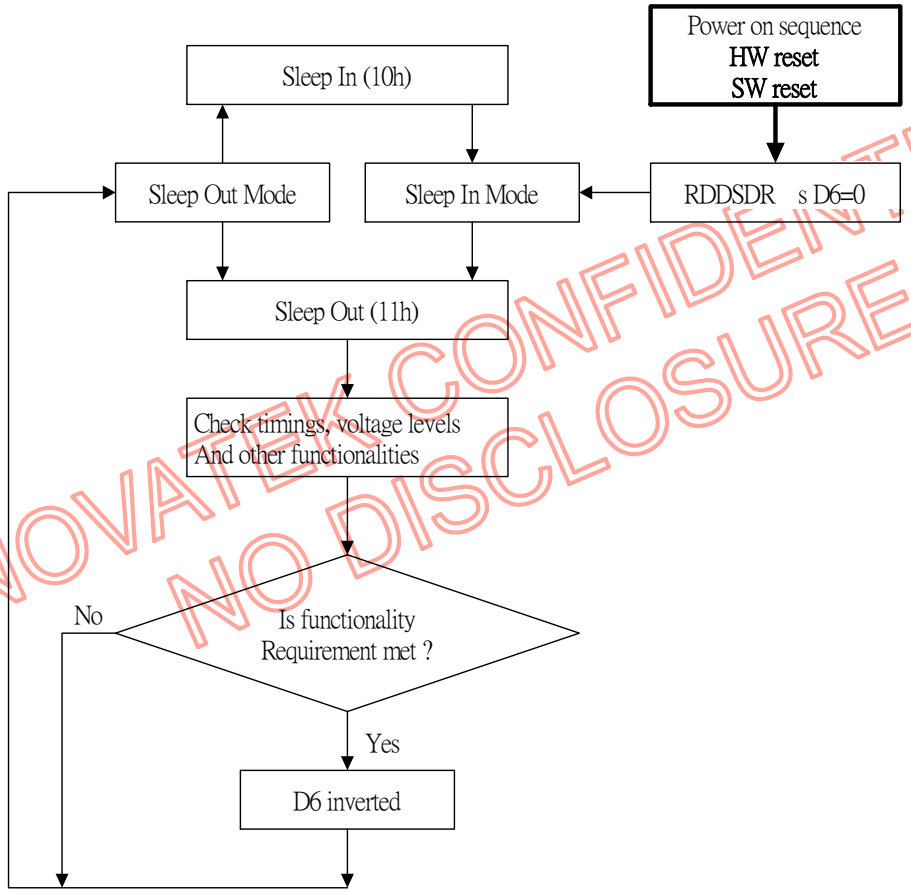
Note: There is not compared and loaded register values, which can be changed by user (00h to AFh and DAh to DDh), by the display module.

5.9.2 Functionality Detection

Sleep Out-command (See section 6.1.12 "Sleep Out (11h)") is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (only Booster voltage level). If functionality requirement is met, there is inverted (= increased by 1) a bit, which defined in command 6.1.10 "Read Display Self- Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1).

The flow chart for this internal function is following:



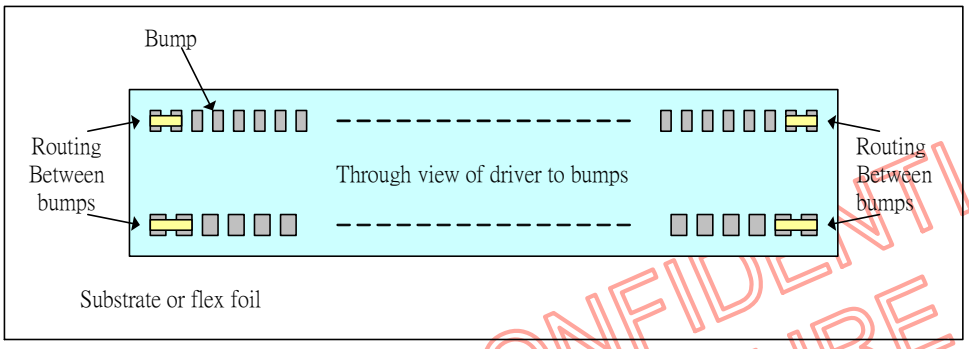
Note: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out –command is sent in Sleep Out -mode.

5.9.3 Chip Attachment Detection

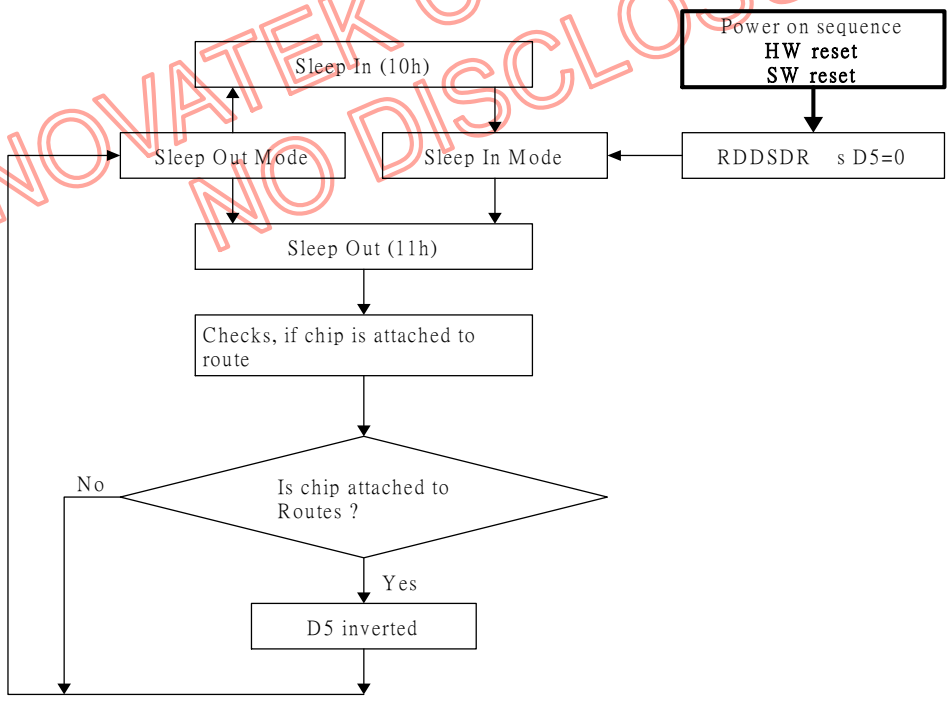
Sleep Out-command (See section 6.1.12 "Sleep Out (11h)") is a trigger for an internal function of the display module, which indicates, if a chip or chips (e.g. driver, etc.) of the display module is/are attached to the circuit route of a flex foil or display glass ITO.

There is inverted (= increased by 1) a bit, which is defined in command 6.1.10 "Read Display Self- Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of this command is D5), if the chip or chips is/are attached to the circuit route of the flex or display glass. If this chip is or those chips are not attached to the circuit route of the flex or display glass, this bit (D5) is not inverted (= increased by 1).

The following figure is for reference purposes; how this chip attachment can be implemented e.g. there are connected together 2 bumps via route of ITO or the flex foil on 4 corners of the driver (chip).



The flow chart for this internal function is following:

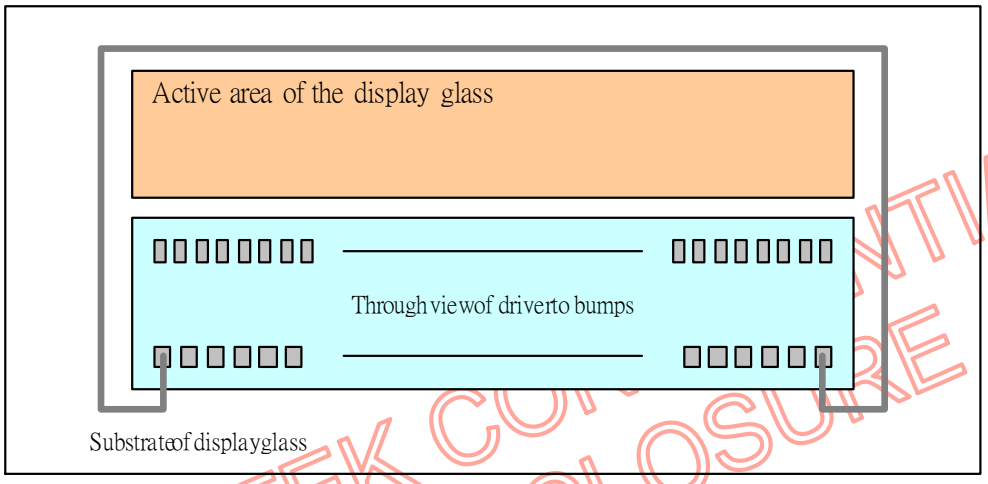


5.9.4 Display Glass Break Detection

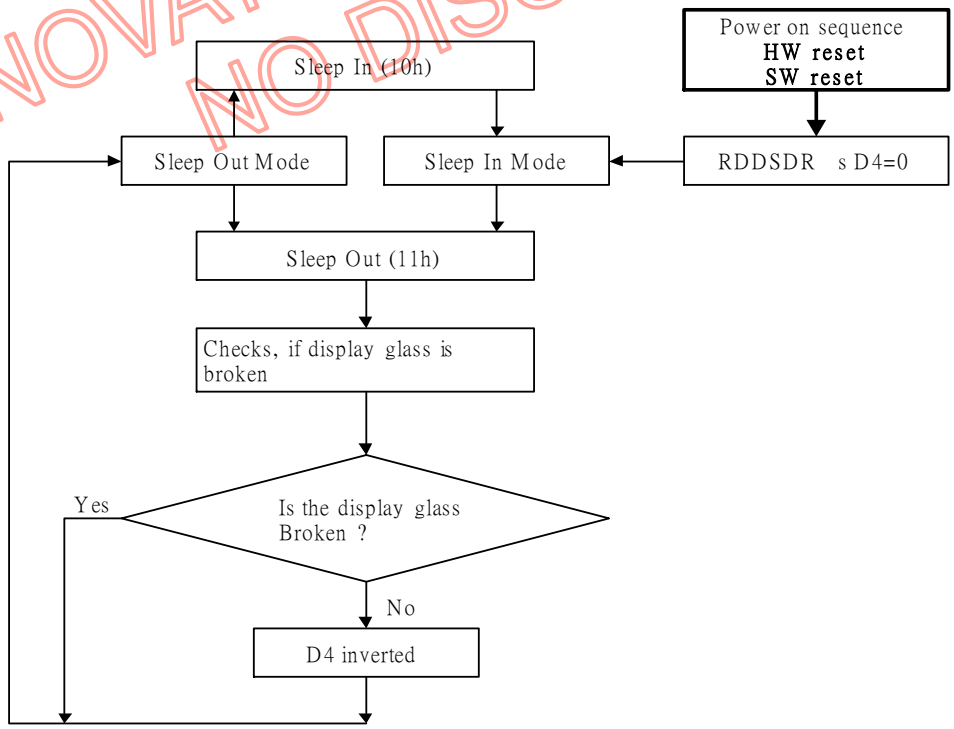
Sleep Out-command (See section 6.1.12 "Sleep Out (11h)") is a trigger for an internal function of the display module, which indicates, if the display glass of the display module is broken or not.

There is inverted (= increased by 1) a bit, which is defined in command 6.1.10 "Read Display Self-Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of this command is D4), if the display glass is not broken. If this display glass is broken, this bit (D4) is not inverted (= increased by 1).

The following figure is a reference, how this glass break detection can be implemented e.g. there is connected together 2 bumps via route of ITO. This route of ITO is the nearest route of the edge of the display glass.



The flow chart for this internal function is following:



5.10 RGB Interface Characteristics

5.10.1 General Timing Diagram

The image information must be correct on the display, when the timings are in range on the interface. However, the image information

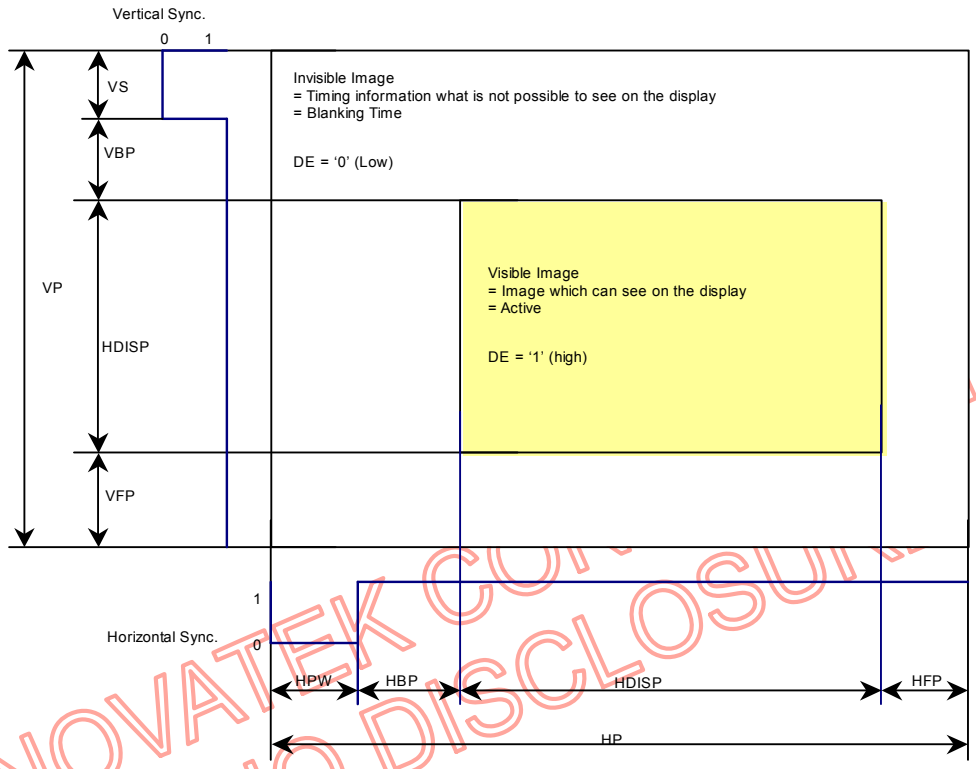


Fig. 7.4.1 RGB General Timing diagram

can be incorrect on the display, when timings are not out of range on the interface (Out of the range timings cannot on the host side). The correct image information must be displayed automatically (by the display module) on the next frame (vertical sync.) when there is returned from out of the range to in range interface timing

5.10.2 Updating Order on Display Active Area (Normal Display Mode On + Sleep Out)

There is defined different kind of updating orders for display. These updating orders are controlled by H/W (SMX, SMY) and S/W (MX, MY, MV) bits

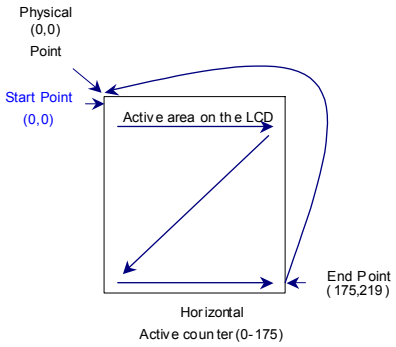


Fig. 7.4.2 Updating order when MADCTLs
MX= '0' and MY= '0'

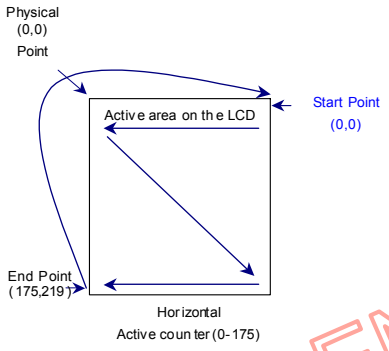


Fig. 7.4.3 Updating order when MADCTLs
MX= '1' and MY= '0'

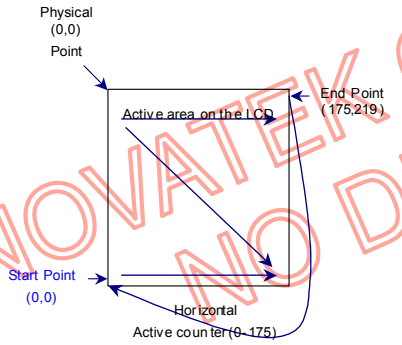


Fig. 7.4.4 Updating order when MADCTLs
MX= '0' and MY= '1'

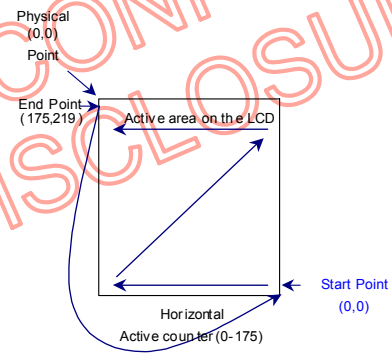
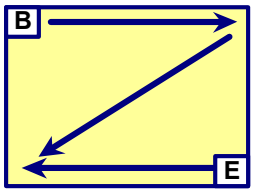


Fig. 7.4.5 Updating order when MADCTLs
MX= '1' and MY= '1'

Table 7.4.1 Rules for Updating Order

Condition	Horizontal Counter	Vertical Counter
An active VS signal is received	Return to 0	Return to 0
Signal Pixel information of the active area is received	Increment by 1	No change
An active HS signal between two active area lines	Return to 0	Increment by 1
The Horizontal counter is larger than 175 and the Vertical counter is larger than 219	Return to 0	Return to 0

Note 1. Pixel order is RGB on the display.
Note 2. Data streaming direction from the host to the display is described in the following figure.
Note 3. In this case, GM="00" and 176RGB x 220.



Data Stream from RGB I/F is like in this figure

Fig. 7.4.6 Data streaming order from RGB I/F

5.10.3 General Timings for RGB I/F

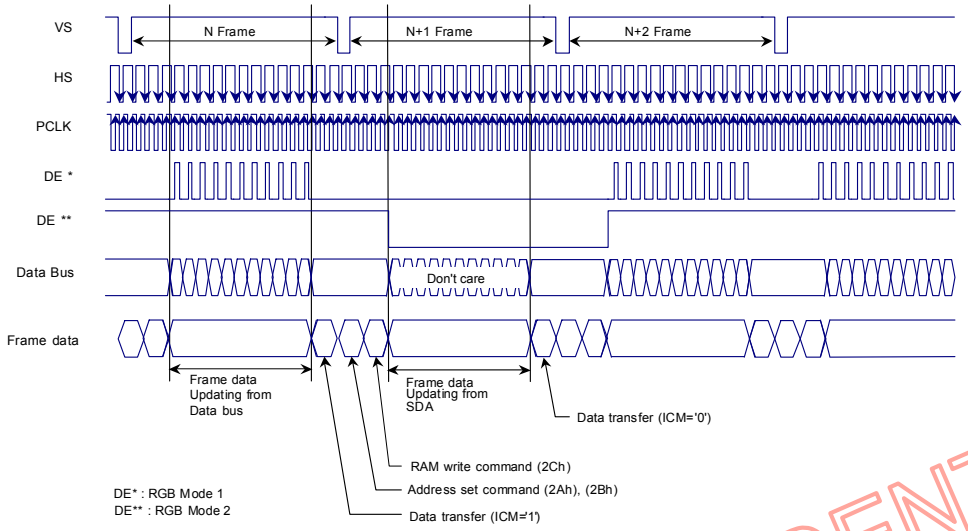


Fig 5.10.3 RAM Access via SPI Interface in RGB mode

5.10.4 Vertical and Horizontal Timings for RGB I/F Mode 1

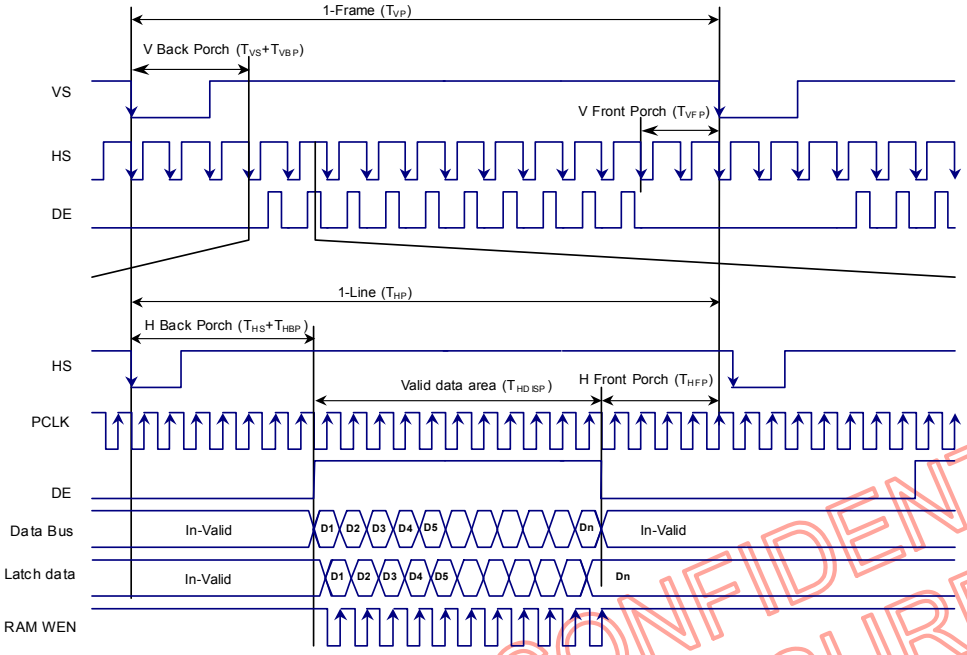
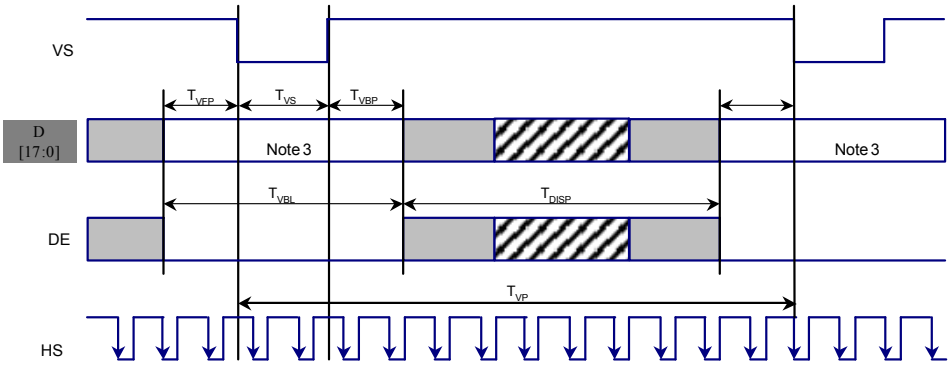


Fig 5.10.4.1 RGB Mode 1 Timing Diagram

Note: DP=0, EP=0, HSP=0 and VSP=0 of RGBCTR (B0h) command.

Vertical Timing for RGB I /F



Horizontal Timing for RGB I/F

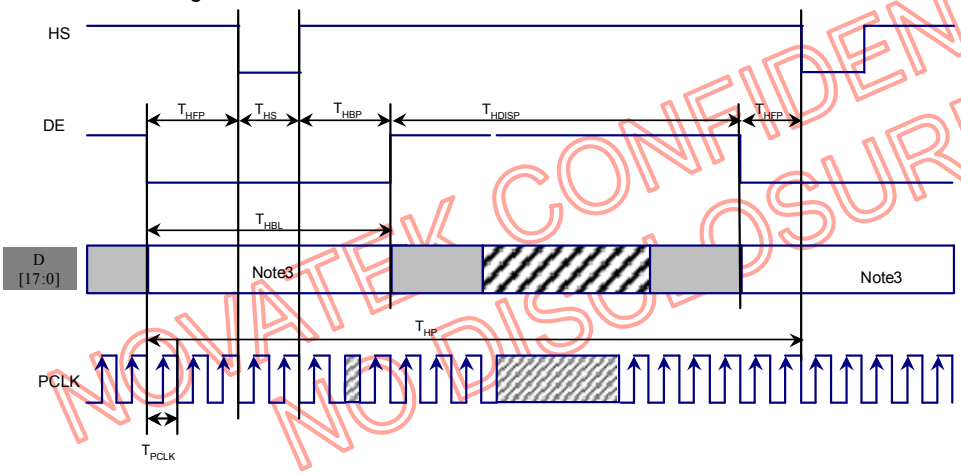


Fig 5.10.4.2 Vertical and Horizontal timing for RGB I/F

Table 5.10.4 Vertical and Horizontal Timing for RGB I/F

Item	Symbol	Condition	Specification			Unit
			Min	Type.	Max	
Vertical Timing						
Vertical cycle period	TVP	GM=00	226		230	HS
		GM=01	182		186	HS
		GM=11	138		142	HS
Vertical low pulse width	TVS		2		4	HS
Vertical front porch	TVFP		2		4	HS
Vertical back porch	TVBP		2		4	HS
Vertical data start line		TVS + TVBP	4		8	HS
Vertical blanking period	TVBL	TVS + TVBP + TVFP	6		10	HS
Vertical active area	TVDISP	GM=00		220		HS
		GM=01		176		HS
		GM=11		132		HS
Vertical refresh rate	TVRR	Frame rate	61.75	65	68.25	Hz
Horizontal Timing						
Horizontal cycle period	THP		208		512	PCLK
Horizontal low pulse width	THS		2		256	PCLK
Horizontal front porch	THFP		2		256	PCLK
Horizontal back porch	THBP		2		256	PCLK
		THS + THBP	30		256	PCLK
Horizontal data start point		ff HS+ fHBP	1.0			μs
Horizontal blanking period	THBL		32		256	PCLK
Horizontal active area	THDISP	GM=00,01,11		176		PCLK
Pixel clock cycle	TPCLKCYC		100		327.3	ns
	fPCLKCYC	TVRR=65Hz	3.0		10	MHz

Note 1. VDDI=1.6 to 3.5V, VDD=2.6 to 3.5V, AGND=DGND=0V, Ta=-30 to 70℃ (to +85℃ no damage)

Note 2. Data lines can be set to High or Low during blanking time Don t care.

Note 3. HP is multiples of eight PCLK.

5.10.5 Vertical and Horizontal Timings for RGB I/F Mode 2

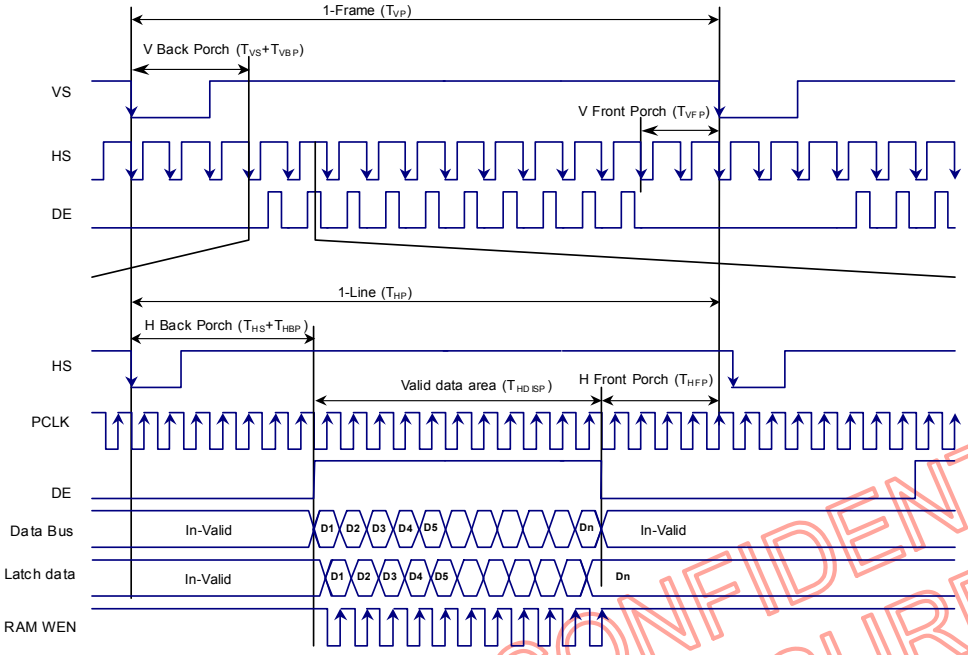
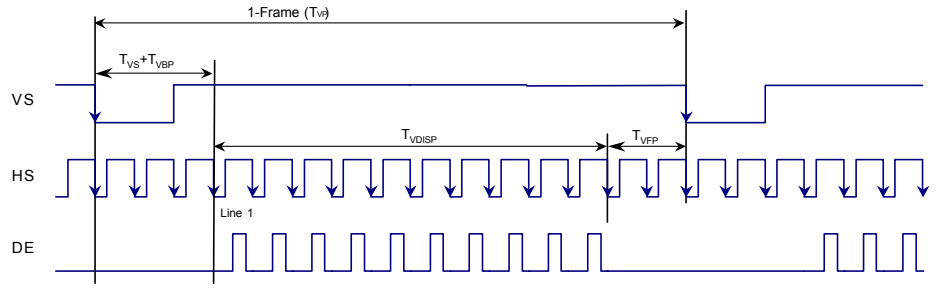


Fig 5.10.5.1 RGB Mode 2 Timing Diagram

Note: DP=0, EP=0, HSP=0 and VSP=0 of RGBCTR (B0h) command.

Vertical Timing for RGB I /F



Horizontal Timing for RGB I/F

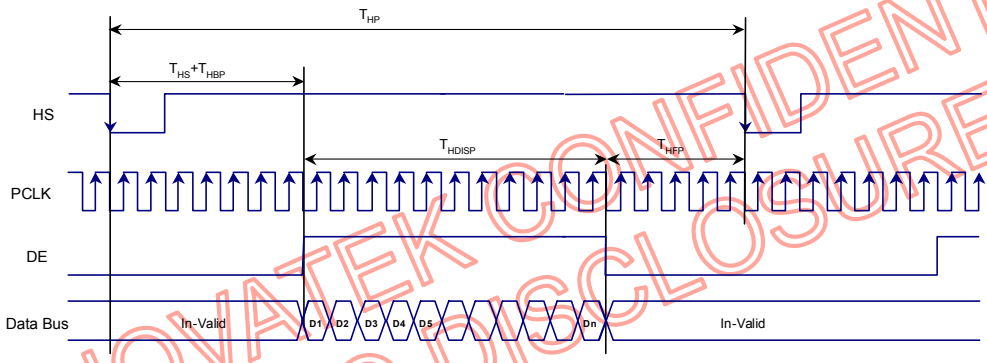


Fig 5.10.5.2 Vertical and Horizontal timing for RGB I/F

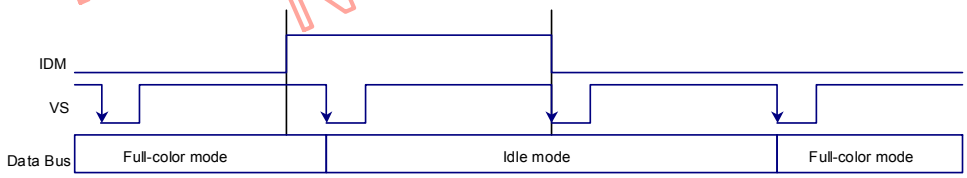


Fig 5.10.5.3 RGB Mode 2 Idle mode Timing Diagram

Table 5.10.5 Vertical and Horizontal Timing for RGB I/F

Item	Symbol	Condition	Specification			Unit
			Min	Type.	Max	
Vertical Timing						
Vertical cycle period	TVP	GM=00	223	224		HS
		GM=01	179	180		HS
		GM=11	135	136		HS
Vertical low pulse width	TVS		1		4	HS
Vertical front porch	TVFP		1	1	1023	HS
Vertical back porch	TVBP		1		1022	HS
Vertical data start line		TVS + TVBP	2	3	1023	HS
Vertical blanking period	TVBL	TVS + TVBP + TVFP	3	4	1023	HS
Vertical active area	TVDISP	GM=00		220		HS
		GM=01		176		HS
		GM=11		132		HS
Vertical refresh rate	TVRR	Frame rate	61.75	65	68.25	Hz
Horizontal Timing						
Horizontal cycle period	THP		179	196	511	PCLK
Horizontal low pulse width	THS		1		63	PCLK
Horizontal front porch	THFP		1	10	63	PCLK
Horizontal back porch	THBP		1		62	PCLK
		THS + THBP	2	10	63	PCLK
Horizontal data start point		ff HS+ fHBP	TBD			μs
Horizontal blanking period	THBL		3	20	256	PCLK
Horizontal active area	THDISP			176		PCLK
Pixel clock cycle	TPCLKCYC		100	350	385	ns
	fPCLKCYC	TVRR=65Hz	2.59	2.85	10.0	MHz

Note 1. VDDI=1.6 to 3.5V, VDD=2.6 to 3.5V, AGND=DGND=0V, Ta=-30 to 70℃ (to +85℃ no damage)

Note 2. Data lines can be set to High or Low during blanking time Don t care.

Note 3. HP is multiples of eight PCLK.

5.10.5.1 Power ON Sequence on RGB I/F Mode 2

The Driver operates power up and display ON by VDD, VDDI, SHUT, VS, HS, DE, PCLK on RGB mode 2 as show as following figure.

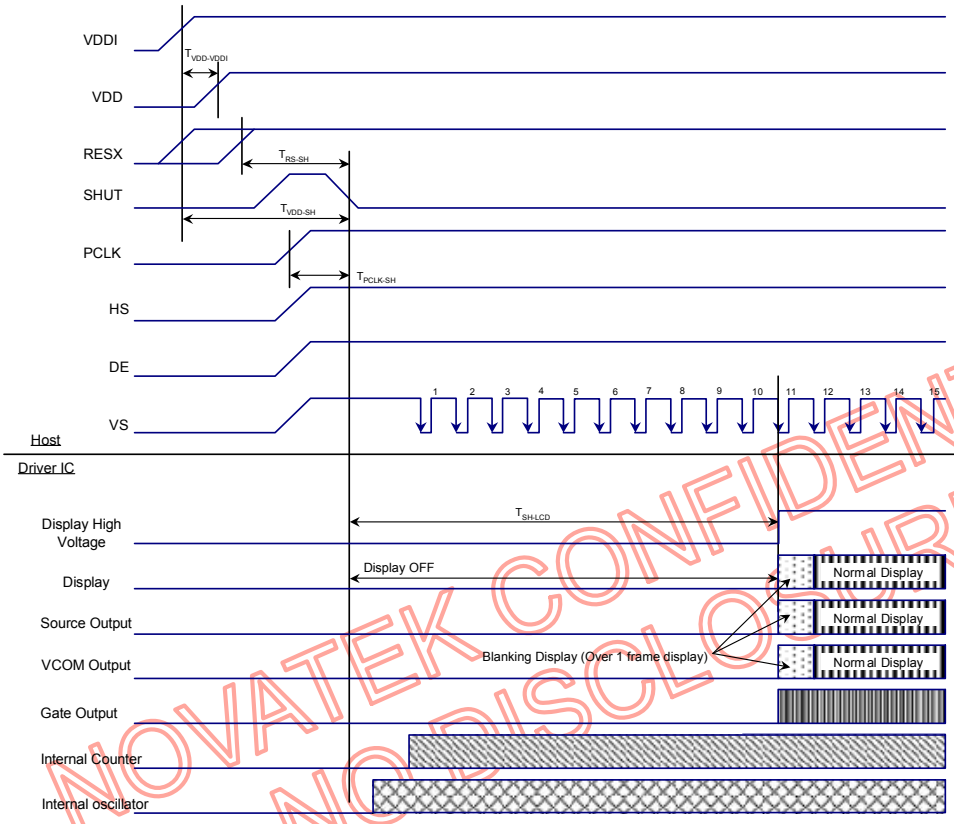


Fig 5.4.5.1 Power ON Sequence on RGB Mode 2

Table 5.4.5.1 Power ON AC Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit	Remark
VDDI On to VDD On	TVDDI-VDD	0			ns	Note1
VDDI/VDD on to falling edge of SHUT	TVDD-SH	1			ms	
RESX to falling of SHUT	TRS-SH	10			us	
Signals input to falling edge of SHUT *	TCLK-SH	1			PCLK	Note2
Falling edge of SHUT to LCD power ON	TSH-LCD			120	ms	
Falling edge of SHUT to Display start	TSH-ON		10		VS	

Note 1: TVDDI-VDD can be <=0ns, >0ns. In any case, VDDI and VDD power up sequence should not have any impact on the driver / display functionalities / performance.
Note 2: Signals mean VS, HS, DE and PCLK signal.
Note 3: DP= 0 , EP= 0 , HSP= 0 and VSP= 0 of RGBCTR (B0h) command.

5.10.5.2 Power OFF Sequence on RGB I/F Mode 2

The Driver operates power off and display OFF by VDD, VDDI, SHUT, VS, HS and DE on RGB mode 2 as show as following figure.

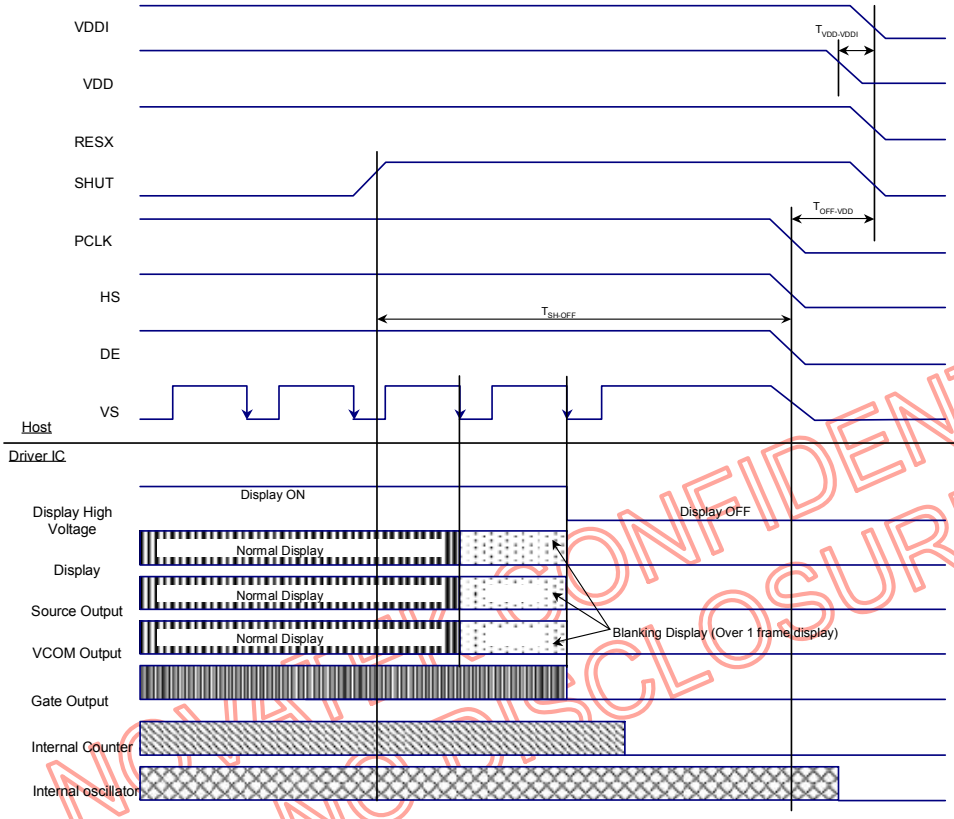


Fig 5.4.5.2 Power OFF Sequence on RGB Mode 2

Table 5.4.5.2 Power OFF AC Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit	Remark
VDDI On to VDD On	$T_{VDDI-VDD}$	0			ns	Note1
Signals input to VDDI/VDD off	T_{SH-OFF}	1			us	Note2
Rising edge of SHUT to Display off	T_{SH-OFF}	2			VS	

Note 1: TVDDI-VDD can be <=0ns, >0ns. In any case, VDDI and VDD power up sequence should not have any impact on the driver / display functionalities / performance.
Note 2: Signals mean VS, HS, DE and PCLK signal.
Note 3: DP= 0 , EP= 0 , HSP= 0 and VSP= 0 of RGBCTR (B0h) command.

5.11 VSYNC Interface

The NT3916 incorporates a VSYNC-I/F, which enables to display a moving picture with only a system interface and frame-synchronizing signal (VS). This interface enables to display moving pictures with minimum modification to a conventional system.

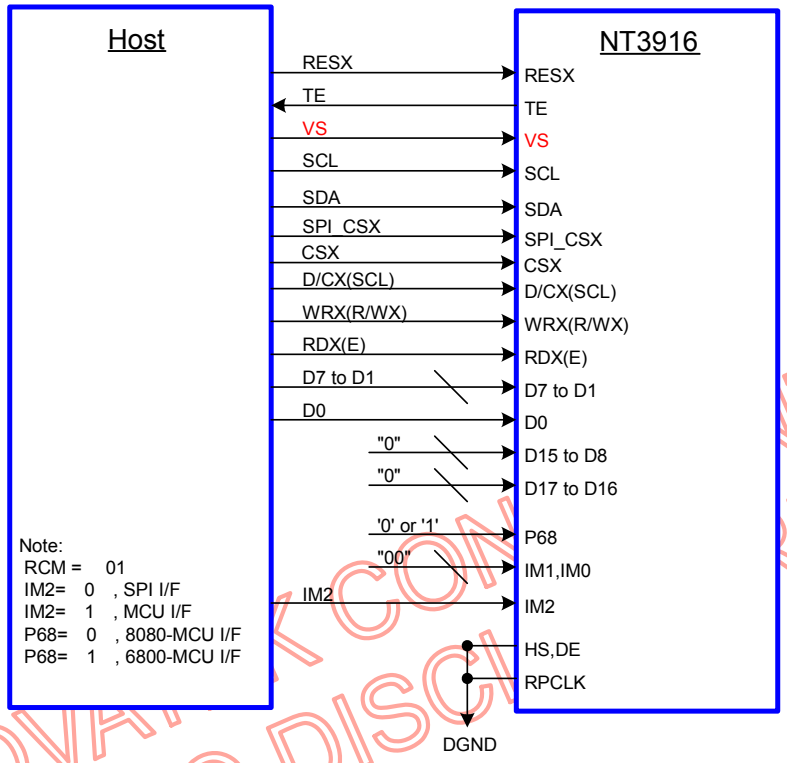
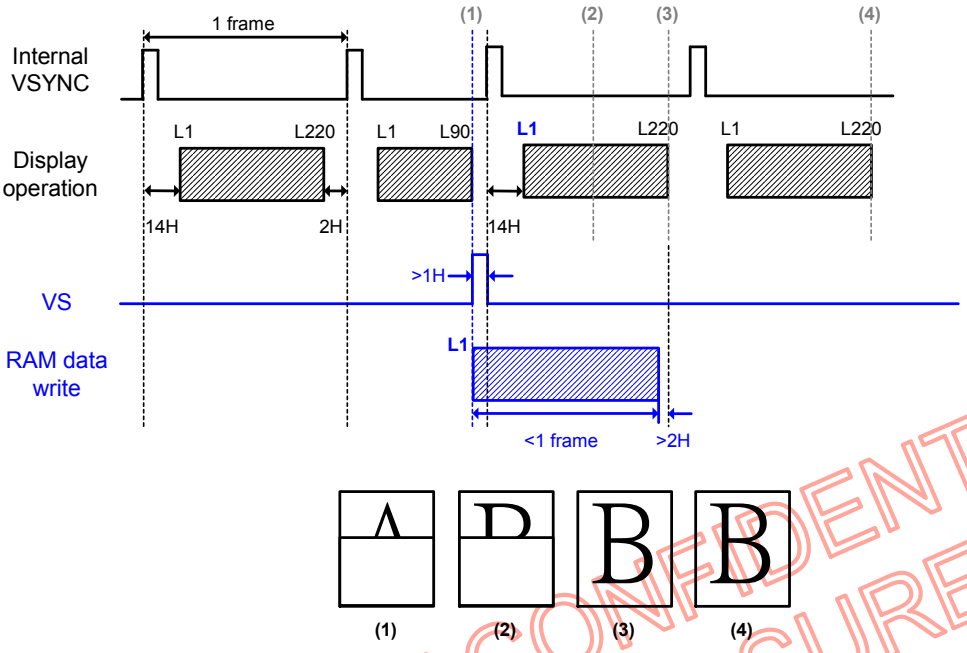


Fig. 5.10.6.1 VSYNC Interface for 8-bits data bus (Example)

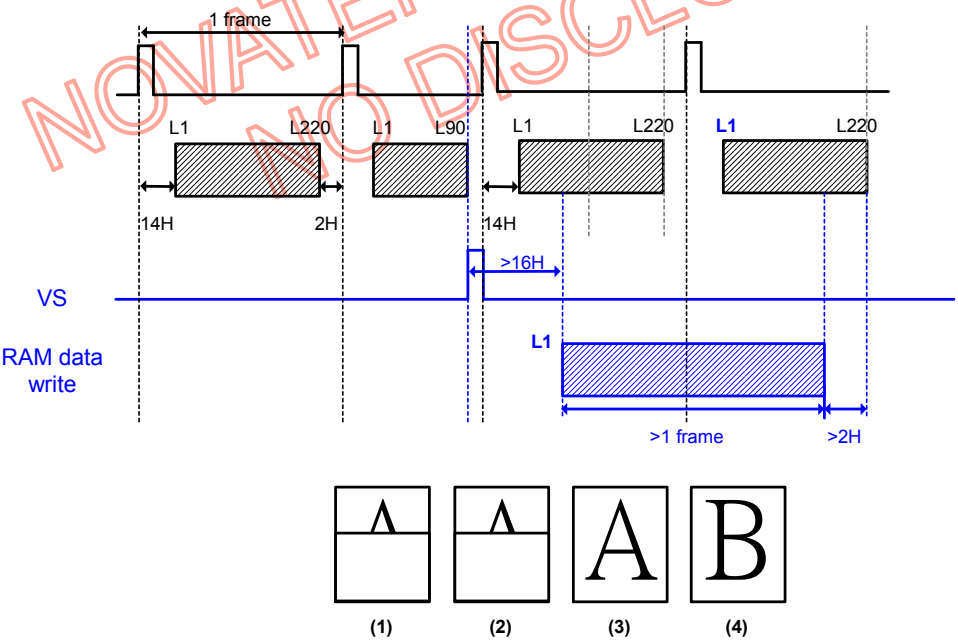
The VSYNC-I/F is truned ON by VSYNC-I/F ON (ADH) command and turned OFF by VSYNC-I/F OFF (ACH) command. In VSYNC-I/F mode, internal display operations are synchronized with VS. The VSYNC-I/F enables to display a moving picture through a system interface and update screens without flicker by writing data to RAM through a system interface in higher speed than the internal display operations by some degree.

The VSYNC-I/F executes display operations only with internal clocks generated by internal oscillators and VS input. All display data are stored in RAM so that only the data relevant to updating a screen are transferred to minimize data transmission while displaying a moving picture.

(1) Leading mode



(2) Lagging mode



The VSYNC-I/F has limits on the minimum RAM write speed through the system interface and the frequency of the internal clocks. It requires a RAM write speed more than the calculated result from the following formula.

- Internal clock frequency (fosc) [Hz]

= Frame Frequency x (DisplayLines +Front Porch(VSFP)+BackPorch (VSBP)) x 16(clocks) x fluctuation

$$\text{RAM Write Speed (Min)(Hz)} = \frac{176 \times \text{Display Line (220 line)}}{(\text{BackPorch(VSBP)} + \text{Display Line - margins}) \times 16(\text{clocks}) \times {}^{1}/_{fosc}}$$

Note 1: When RAM write does not start right after the falling edge of VS, the time from the falling edge of VS until RAM write starts must also be taken into account.

An example of RAM write speed and the frequency of the internal clocks in VSYNC-I/F mode is as follows.

Example:

Display size: 176 RGB × 220 lines

Raster-rows: 220 lines

Back/ Front porch: 14/ 2 lines (VSBP = 1110/ VSFP = 0010 of AFh)

-When Frame frequency: 65Hz

Internal clock frequency (fosc) [Hz]

= 65 Hz × (220+2+14) lines × 16 Clocks × 1.1 / 0.9 = 300kHz

-When Frame frequency: 60 Hz

Internal clock frequency (fosc) [Hz]

= 60Hz × (220+2+14) lines × 16 Clocks × 1.1 / 0.9 = 277kHz

When calculating an internal clock frequency, possible causes of fluctuations must also be taken into consideration. In this example, the allowance for the fluctuation is ± 10 % from the center value, and the frequency must be within a VS cycle.

Also in this example, variations attributed to LSI fabrication and room temperature are taken into consideration as causes of fluctuations. Other possible causes of fluctuations, such as variations in external resistors or voltage changes are not considered in this example. It is necessary to make a setting with enough margins to accommodate

-When Frame frequency: 65Hz

Minimum speed for RAM writing [Hz] >

176 × 220 / {(14 + 220 - 2) lines × 16 clock) / 300 kHz} = 3.13MHz

-When Frame frequency: 60Hz

Minimum speed for RAM writing [Hz] >

176 × 220 / {(14 + 220 - 2) lines × 16 clock) / 300 kHz} = 2.89MHz

Note 2: The above calculation is premised on the case of writing data to RAM on the falling edge of VS.

Note 3: There must at least be a margin of 2 processing lines when all one-frame data are written to RAM before the NT3916 starts processing display lines.

By writing data to RAM on falling edge of VS at speed of 2.89MHz (Frame rate=60Hz) or more, it is possible to overwrite an entire screen without flicker by completing data write operation of a line before it starts display operation of that line.

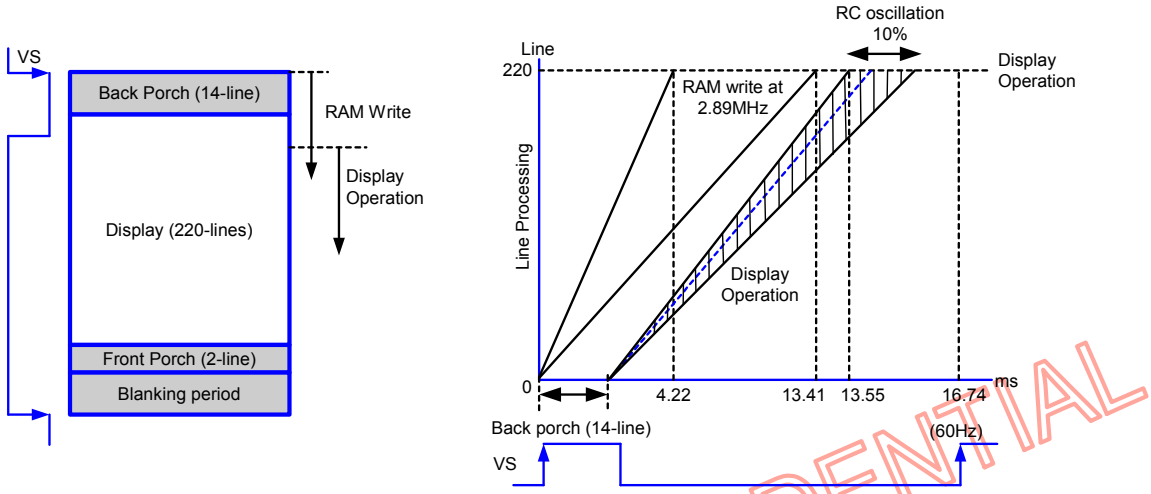
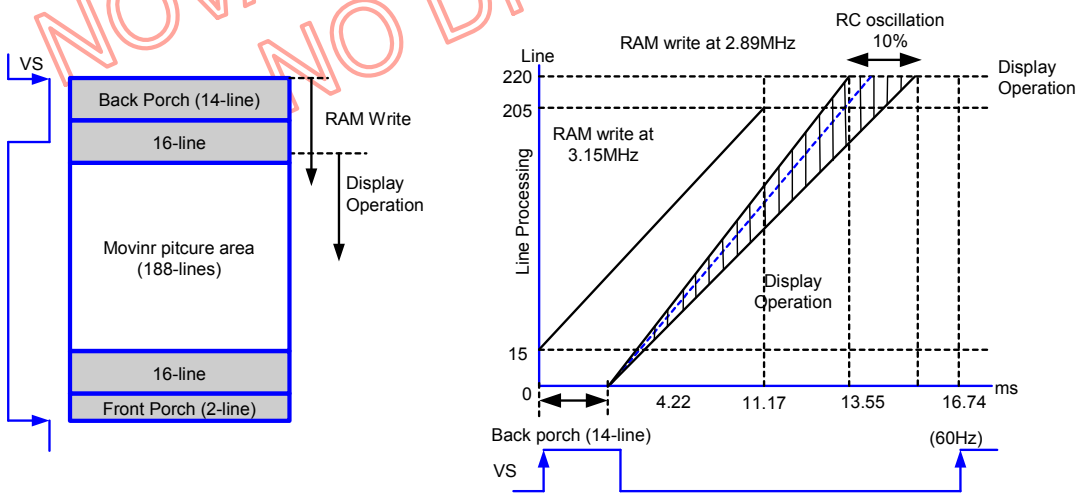


Fig. 5.10.6.2 Operation via VSYNC-I/F

Notes to the VSYNC Interface

1. The aforementioned example of calculation is just a result of calculation. In actual settings, possible causes of fluctuations such as variations in internal oscillators should be taken into consideration. It is necessary to give enough margins when setting RAM write speed.

2. The aforementioned example of calculation is the value in case of overwriting full screen. If a moving picture display area is limited, it will result in more margins between RAM write and display operations.



3. A front porch period continues after completion of 1 frame and until the next input of VS.

5.12 VSYNC Interface display Data Format

- 8-Bits Parallel Interface (IM1, IM0= “00”)

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	**2Ch**
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
03h	x	x	x	x	x	x	x	x	x	x	R3	R2	R1	R0	G3	G2	G1	G0	4K-Colour (2-pixels/ 3-byyes)
	x	x	x	x	x	x	x	x	x	x	B3	B2	B1	B0	R3	R2	R1	R0	
	x	x	x	x	x	x	x	x	x	x	G3	G2	G1	G0	B3	B2	B1	B0	
05h	x	x	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	65K-Colour (1-pixels/ 2-byyes)
	x	x	x	x	x	x	x	x	x	x	G2	G1	G0	B4	B3	B2	B1	B0	
06h	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Colour (1-pixels/ 3byyes)
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

- 16-Bits Parallel Interface (IM1, IM0= “01”)

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	**2Ch**
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
03h	x	x	x	x	x	x	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0	4K-Colour
05h	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	65K-Colour
06h	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	262K-Colour (2-pixels/ 3byyes)
	x	x	B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x	
	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x	

- 9-Bits Parallel Interface (IM1, IM0= “10”)

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	**2Ch**
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
06h	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Colour (1-pixels/ 2byyes)
	x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

- 18-Bits Parallel Interface (IM1, IM0= “11”)

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	**2Ch**
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
03h	x	x	x	x	x	x	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0	**4K-Colour**
05h	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	**65K-Colour**
06h	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	**262K-Colour**

6. COMMAND

6.1 System function Command List and Description

Table 6.1.1 System Function command List (1)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
NOP	6.1.1	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)	No Operation
SWRESET	6.1.2	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)	Software reset
RDDID	6.1.3	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)	Read Display ID
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	38h	ID1 read
		1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	8xh	ID2 read
		1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	62h	ID3 read
RDDST	6.1.4	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)	Read Display Status
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24	00h	-
		1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON	61h	-
		1	1	↑	-	VSSON	ST14	INVON	ST12	ST11	DISON	TEON	GCS2	00h	-
		1	1	↑	-	GCS1	GCS0	TELOM	HSON	VSON	PCKON	DEON	ST0	00h	-
RDDPM	6.1.5	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)	Read Display Power Mode
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	D1	D0	08h	-
RDD MADCTR	6.1.6	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)	Read Display MADCTR
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	MX	MY	MV	ML	RGB	MH	D1	D0	00h	-
RDD COLMOD	6.1.7	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)	Read Display Pixel Format
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	VIPF3	VIPF2	VIPF1	VIPF0	D3	IFPF2	IFPF1	IFPF0	66h	-
RDDIM	9.1.8	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)	Read Display Image Mode
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	VSSON	D6	INVON	D4	D3	GCS2	GCS1	GCS0	00h	-
RDDSM	6.1.9	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)	Read Display Signal Mode
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	TEON	TELOM	HSON	VSON	PCKON	DEON	D1	D0	00h	-
RDDSDR	6.1.10	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)	Read Display Self-diagnostic result
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	RELD	FUND	ATTD	BRD	D3	D2	D1	D0	00h	-

"-": Don't care

Table 6.1.1 System Function command List (2)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
SLPIN	6.1.11	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)	Sleep in & booster off
SLPOUT	6.1.12	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)	Sleep out & booster on
PTLON	6.1.13	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)	Partial mode on
NORON	6.1.14	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)	Partial off (Normal)
INVOFF	6.1.15	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)	Display inversion off (normal)
INVON	6.1.16	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)	Display inversion on
GAMSET	6.1.17	0	↑	1	-	0	0	1	0	0	1	1	0	(26h)	Gamma curve select
		1	↑	1	-	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	01h	-
DISPOFF	6.1.18	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)	Display off
DISPON	6.1.19	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)	Display on
CASET X=7Fh,	6.1.20	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)	Column address set
		1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	00h	X address start: 0 ≤XS ≤X
		1	↑	1	-	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	00h	
		1	↑	1	-	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	00h	X address end: XS ≤XE ≤X
		1	↑	1	-	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	EFh	
RASET Y=9Fh	6.1.21	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)	Row address set
		1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	00h	Y address start: 0 ≤ YS ≤ Y
		1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	00h	
		1	↑	1	-	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	01h	Y address end: YS ≤ YE ≤ Y
		1	↑	1	-	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	3Fh	
RAMWR	6.1.22	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)	Memory write
		1	↑	1	D17-8	D7	D6	D5	D4	D3	D2	D1	D0		Write data
RAMHD	6.1.23	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)	Memory read
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	D17-8	D7	D6	D5	D4	D3	D2	D1	D0		Read data
RGBSET a = 31, b = 63, c = 31	6.1.24	0	↑	1	-	0	0	1	0	1	1	0	1	(2Dh)	LUT for 65k , 262K color display
		1	↑	1	-	-	-	R005	R004	R003	R002	R001	R000		Red tone 0
		1	↑	1	:	:	:	:	:	:	:	:	:		: -
		1	↑	1	-	-	-	Ra5	Ra4	Ra3	Ra2	Ra1	Ra0		Red tone "a"
		1	↑	1	-	-	-	G005	G004	G003	G002	G001	G000		Green tone 0
		1	↑	1	:	:	:	:	:	:	:	:	:		: -
		1	↑	1	-	-	-	Gb5	Gb4	Gb3	Gb2	Gb1	Gb0		Green tone "b"
		1	↑	1	-	-	-	B005	B004	B003	B002	B001	B000		Blue tone 0
		1	↑	1	:	:	:	:	:	:	:	:	:		: -
		1	↑	1	-	-	-	Bc5	Bc4	Bc3	Bc2	Bc1	Bc0		Blue tone "c"

"-": Don't care

Table 6.1.1 System Function command List (3)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
PTLAR	6.1.25	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)	Partial start/end address set
		1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	00h	Partial start address (0,1,2, .., P)
		1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	00h	
		1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	00h	Partial end address (0,1,2, .., P)
		1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0		
SCRLAR	6.1.26	1	↑	1	-	0	0	1	1	0	0	1	1	(33h)	Scroll area set
		1	↑	1	-	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8	00h	Top fixed area (0,1,2, .., S)
		1	↑	1	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	00h	
		1	↑	1	-	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8	00h	Vertical scroll area (0,1,2, .., S)
		1	↑	1	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0		
		1	↑	1	-	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8	00h	Bottom fixed area (0,1,2, .., S)
		1	↑	1	-	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	00h	
TEOFF	6.1.27	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)	Tearing effect line off
TEON	6.1.28	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)	Tearing effect mode set & on
		1	↑	1	-	0	0	0	0	0	0	0	M	00h	M='0": Mode1, M="1": Mode2
MADCTR	6.1.29	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)	Memory data access control
		1	↑	1	-	MY	MX	MV	ML	RGB	MH	0	0	00h	-
VSCSAD V=159	6.1.30	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)	Scroll start address of RAM
		1	↑	1	-	SSA15	SSA14	SSA13	SSA12	SSA11	SSA10	SSA9	SSA8	00h	SSA = 0, 1, 2, …, V
		1	↑	1	-	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	00h	
IDMOFF	6.1.31	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)	Idle mode off
IDMON	6.1.32	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)	Idle mode on
COLMOD	6.1.33	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)	Interface pixel format
		1	↑	1	-	VIPF3	VIPF2	VIPF1	VIPF0	0	IFPF2	IFPF1	IFPF0	66h	Interface format
RDID1	6.1.34	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)	Read ID1
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	38h	Read parameter
RDID2	6.1.35	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)	Read ID2
		1	1	↑			-	-	-	-	-	-	-		Dummy read
		1	1	↑		ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	8xh	Read parameter
RDID3	6.1.36	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)	Read ID3
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	62h	Read parameter
SRGBOFF	6.1.37	0	↑	1	-	1	0	1	0	1	0	1	0	(AAh)	Separate gamma control off
SRGBON	6.1.38	0	↑	1	-	1	0	1	0	1	0	1	1	(ABh)	Separate gamma control on
VSYNCOFF	6.1.39	0	↑	1	-	1	0	1	0	1	1	0	0	(ACh)	VSYNC Interface off
VSYNCON	6.1.40	0	↑	1	-	1	0	1	0	1	1	0	1	(ADh)	VSYNC Interface on
VSCTR1	6.1.41	0	↑	1	-	1	0	1	0	1	1	1	0	(AEh)	VSYNC Interface control
		1	↑	1		VSFP3	VSFP2	VSFP1	VSFP0	VSBP3	VSBP2	VSBP1	VSBP0	E2h	

"-": Don't care

Note 1. After the H/W reset by RESX pin or S/W reset by SWRESET command, each internal register becomes default state (Refer "RESET TABLE" section)

Note 2. Undefined commands are treated as NOP (00 h) command.

Note 3. B0 to D9 and DE to FF are for factory use of driver supplier.

Note 4. Commands 10h, 12h, 13h, 20h, 21h, 26h, 28h, 29h, 30h, 33h, 36h (ML parameter only), 37h, 38h and 39h are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09h), Read Display Power Mode (0Ah), Read Display MADCTR (0Bh), Read Display Pixel Format (0Ch), Read Display Image Mode (0Dh), Read Display Signal Mode (0Eh) and Read Display Self Diagnostic Result (0Fh) of these commands are updated immediately both in Sleep In mode and Sleep Out mode.

6.1.1 NOP (00h)

00H	NOP (No Operation)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)
Parameter	No Parameter												-

NOTE: "-" Don't care

Description	-This command is empty command. It does not have effect on the display module. -However it can be used to terminate RAM data write or read as described in RAMWR (Memory Write), RAMRD (Memory Read) and parameter write commands.
Restriction	-
Register Availability	Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes
Default	Status: Power On Sequence — Default Value: N/A Status: S/W Reset — Default Value: N/A Status: H/W Reset — Default Value: N/A
Flow Chart	-

6.1.2 SWRESET (01h): Software Reset

01H	SWRESET (Software Reset)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)
Parameter	No Parameter												

NOTE: "-" Don't care

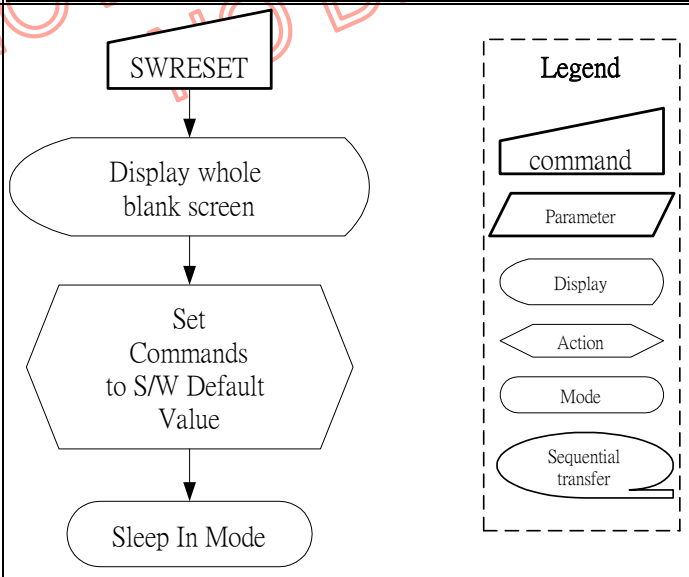
Description	-When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values and all source & gate outputs are set to VSS (display off). (See default tables in each command description) *Note: The Frame Memory contents are not affected by this command.*
Restriction	-It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display supplier's factory default values to the registers during 5msec. -If Software Reset is applied during Sleep Out mode, it will be necessary to wait *120msec* before sending Sleep Out command. -Software Reset command cannot be sent during Sleep Out sequence.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart



6.1.3 RDDID (04h): Read Display ID

04H	RDDID (Read Display ID)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)
Dummy Read	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-
3rd parameter	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-
4th parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-

NOTE: "-" Don't care

Description

-This read byte returns 24-bit display identification information.
-The 1stparameter is dummy data
-The 2ndparameter (ID17 to ID10): LCD module's manufacturer ID.
-The 3rdparameter (ID27 to ID20): LCD module/driver version ID.
-The 4th parameter (ID37 to UD30): LCD module/driver ID.
NOTE: Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 2,3,4 of the command 04h, respectively.

Restriction

-

Register Availability

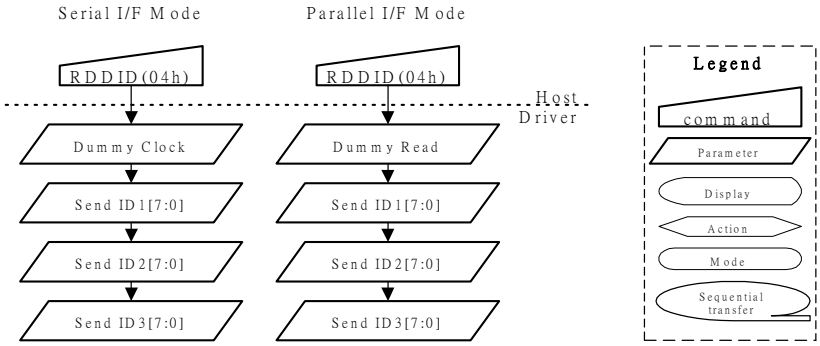
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	ID1	ID2	ID3
Power On Sequence	38h	MTP	MTP
S/W Reset	38h	MTP	MTP
H/W Reset	38h	MTP	MTP

Note: ID1 can be modified by metal option.

Flow Chart



6.1.4 RDDST (09h): Read Display Status

09H	RDDST (Read Display Status)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24	00h
3rd Parameter	1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON	61h
4th Parameter	1	1	↑	-	VSSON	ST14	INVON	ST12	ST11	DISON	TEON	GCS2	00h
5th Parameter	1	1	↑		GCS1	GCS0	TELOM	HSON	VSON	PCKON	DEON	ST0	00h

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
BSTON	Booster Voltage Status	"1"=Booster on,"0"= Booster off,
MY	Row Address Order (MY)	"1"=Decrement, (Bottom to Top, when MADCTL (36h) D7='1') "0"=Increment, (Top to Bottom, when MADCTL (36h) D7='0')
MX	Column Address Order (MX)	"1"=Decrement, (Right to Left, when MADCTL (36h) D6='1') "0"=Increment, (Left to Right, when MADCTL (36h) D6='1')
MV	Row/Column Exchange (MV)	"1"= Row/column exchange, (when MADCTL (36h) D5='1') "0"= Normal (MV=0), (when MADCTL (36h) D5='0')
ML	Vertical refresh Order (ML)	"1"=Decrement, (LCD refresh Bottom to Top, when MADCTL (36h) D4='1') "0"=Increment, (LCD refresh Top to Bottom, when MADCTL (36h) D4='0')
RGB	RGB/BGR Order (RGB)	"1"=BGR, (When MADCTL (36h) D3='1') "0"=RGB, (When MADCTL (36h) D3='0')
MH	Horizontal refresh Order (MH)	"1"=Decrement, (LCD refresh Right to Left, when MADCTL (36h) D2='1') "0"=Increment, (LCD refresh Left to Right, when MADCTL (36h) D2='0')
ST24	Not Used	"0"
ST23	Not Used	"0"
IFPF2	Interface Color Pixel Format Definition	"011" = 12-bit / pixel "101" = 16-bit / pixel, "110" = 18-bit / pixel,

ST21			
ST20			
	IDMON	Idle Mode On/Off	"1" = On, "0" = Off
	PTLON	Partial Mode On/Off	"1" = On, "0" = Off
	SLOUT	Sleep In/Out	"1" = Out, "0" = In
	NORON	Display Normal Mode On/Off	"1" = Normal Display, "0" = Normal Display off
	VSSON	Vertical Scrolling Status	"1" = Scroll on, "0" = Scroll off
	ST14	Horizontal Scroll Status	"0"
	INVON	Inversion Status	"1" = On, "0" = Off
	ST12	All Pixels On (Not Used)	"0"
	ST11	All Pixels Off (Not Used)	"0"
	DISON	Display On/Off	"1" = On, "0" = Off
	TEON	Tearing effect line on/off	"1" = On, "0" = Off
	GCS2 GCS1	Gamma Curve Selection	"000" = GC0 (Gamma 2.2) "001" = GC1 (Gamma 1.8) "010" = GC2 (Gamma 2.5) "011" = GC3 (Gamma 1) "100" to "111" = Not defined
ST6			
TELOM	Tearing effect line mode	"0" = mode1, "1" = mode2	
HSON	Horizontal Sync. (HS, RGB I/F)	'1' = On, '0' = Off	
VSON	Vertical Sync, (VS, RGB I/F)	'1' = On, '0' = Off	
PCKON	Pixel Clock (PCLK, RGB I/F)	'1' = On, '0' = Off	
DEON	Data Enable (DE, RGB I/F)	'1' = On, '0' = Off	
ST0	For Future Use	"0"	

	Note: ST0, ST5, ST9, ST11-ST15, ST19, ST23, ST24 are set to '0', when RGB I/F.

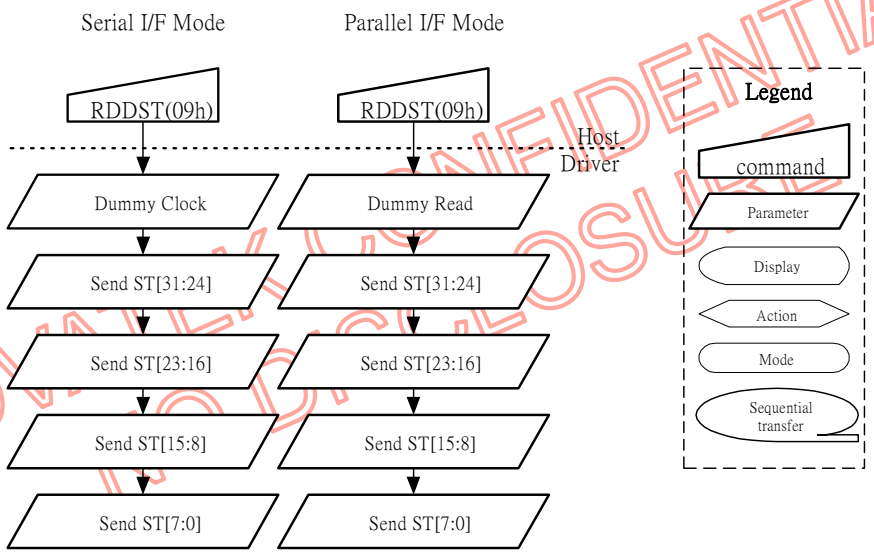
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (ST31 to ST0):			
	ST[31-24]	ST[23-16]	ST[15-8]	ST[7-0]
Power On Sequence	0000-0000	0110-0001	0000-0000	0000-0000
S/W Reset	0xxx-xx00	0xxx-0001	0000-0000	0000-0000
H/W Reset	0000-0000	0110-0001	0000-0000	0000-0000

Flow Chart



6.1.5 RDDPM (0Ah): Read Display Power Mode

0AH	RDDPM (Read Display Power Mode)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑		BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	D1	D0	08h

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value	
BSTON	Booster Voltage Status	"1"=Booster on,	"0"=Booster off
IDMON	Idle Mode On/Off	"1" = Idle Mode On,	"0"= dle Mode Off
PTLON	Partial Mode On/Off	"1" = Partial Mode On,	"0" = Partial Mode Off
SLPOUT	Sleep In/Out	"1" = Sleep Out,	"0" = Sleep In
NORON	Display Normal Mode On/Off	"1" = Normal Display,	"0" = Partial Display
DISON	Display On/Off	"1" = Display On,	"0" = Display Off
D1	Not Used	"0"	
D0	Not Used	"0"	

Restriction

-

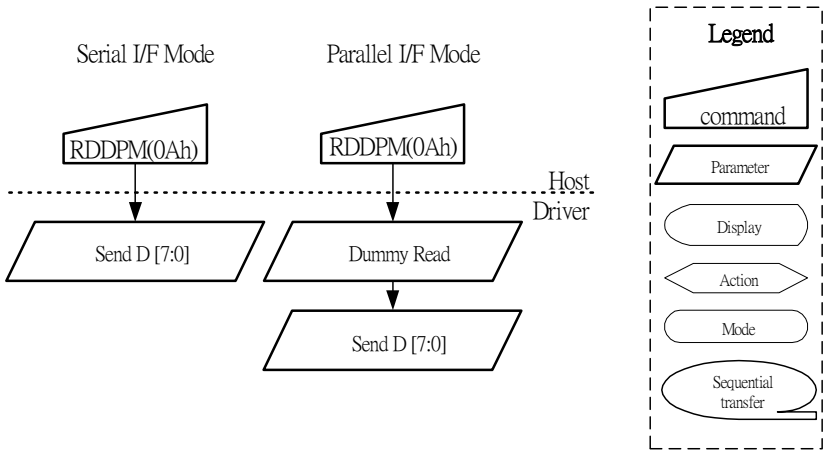
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	08h (0000_1000)
S/W Reset	08h (0000_1000)
H/W Reset	08h (0000_1000)

Flow Chart



6.1.6 RDDMADCTR (0Bh): Read Display MADCTR

0BH	RDDMADCTR (Read Display MADCTR)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDMADCTR	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑		MX	MY	MV	ML	RGB	MH	D1	D0	00h

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
MX	Row Address Order	"1"=Decrement, "0"=Increment
MY	Column Address Order	"1"=Decrement, "0"=Increment
MV	Row/Column Order (MV)	"1"= Row/column exchange (MV=1) "0"= Normal (MV=0)
ML	Scan Address Order	'1' =LCD Refresh Top to Bottom '0' =LCD Refresh Bottom to Top
RGB	RGB/BGR Order	"1"=BGR, "0"=RGB
MH	Display data latch order	'1' =LCD Refresh left to right '0' =LCD Refresh left to right
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

-

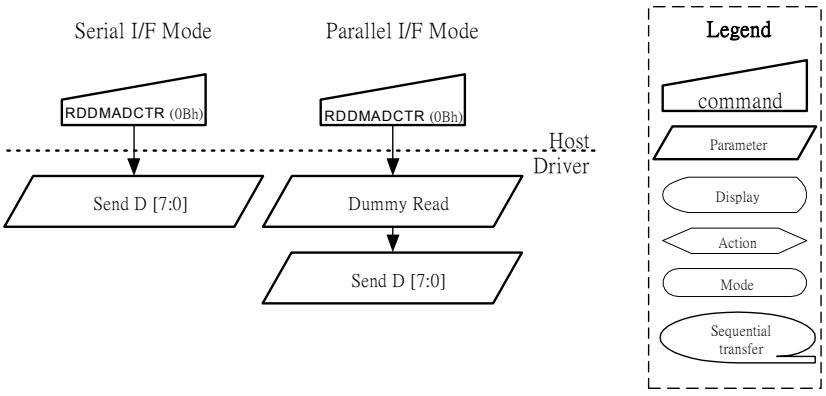
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h (0000_0000)
S/W Reset	No change

Flow Chart



6.1.7 RDDCOLMOD (0Ch): Read Display Pixel Format

0CH	RDDCOLMOD (Read Display Pixel Format)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDCOLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	VIPF3	VIPF2	VIPF1	VIPF0	D3	IFPF2	IFPF1	IFPF0	66h

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
VIPF3 VIPF2 VIPF1 VIPF0	RGB Interface Color Format	"0101"=16 bit/pixel (1 times data transfer) "0110"=18 bit/pixel (1 times data transfer) "1110"=6 bit/pixel (3 times data transfer) The others = not defined
D3		"0" (Not Used)
IFPF2	Control Interface Color Format	"011"=12 bit/pixel (RGB 4,4,4-bits) "101"=16 bit/pixel (RGB 5,6,5-bits) "110"=18 bit/pixel (RGB 6,6,6-bits) The others = not defined
D1		
D0		

Restriction

-

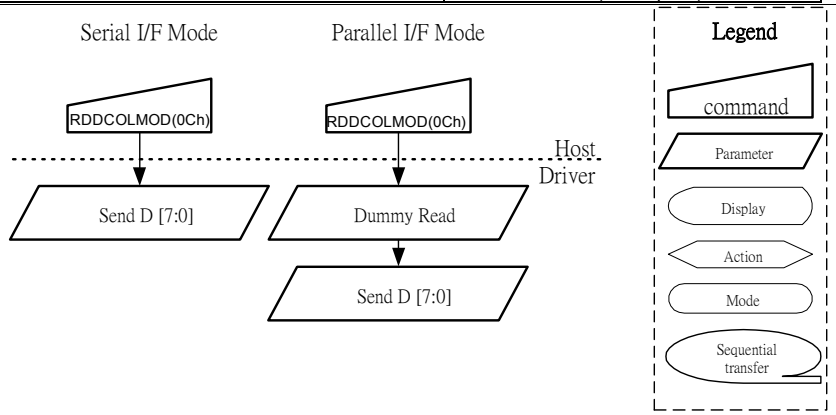
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	66h (18 bit/pixel)
S/W Reset	No Change
H/W Reset	66h (18 bit/pixel)

Flow Chart



6.1.8 RDDIM (0Dh): Read Display Image Mode

0DH	RDDIM (Read Display Image Mode)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	VSSON	D6	INVON	D4	D3	GCS2	GCS 1	GCS 0	00h

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
VSSON	Vertical Scrolling On/Off	"1" = Vertical scrolling is On, "0" = Vertical scrolling is Off
D6	Horizontal Scrolling On/Off	"0" (Not used)
INVON	Inversion On/Off	"1" = Inversion is On, "0" = Inversion is Off
D4	All Pixels On	"0" (Not used)
D3	All Pixels Off	"0" (Not used)
GCS2	Gamma Curve Selection	"000" = GC0 (Gamma 2.2) "001" = GC1 (Gamma 1.8) "010" = GC2 (Gamma 2.5) "011" = GC3 (Gamma 1.0) "100" to "111" = Not defined
GCS1		
GCS0		

Restriction

-

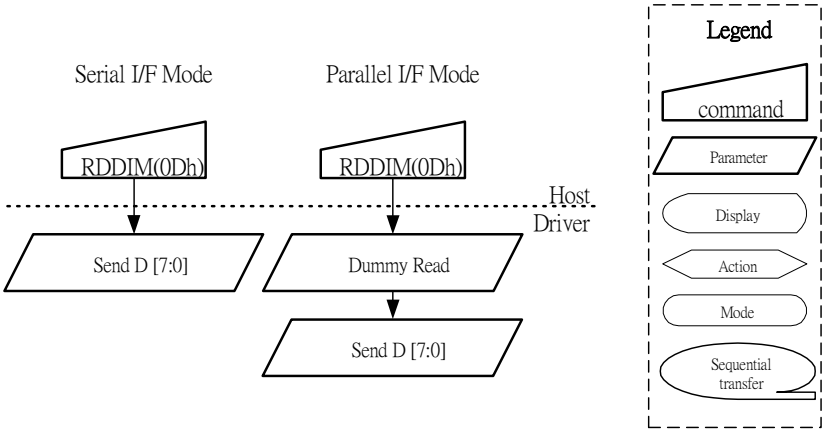
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h (0000_0000)
S/W Reset	00h (0000_0000)

Flow Chart



6.1.9 RDDSM (0Eh): Read Display Signal Mode

0EH	RDDSM (Read Display Signal Mode)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	TEON	TELOM	HSON	VSON	PCKON	DEON	D1	D0	00h

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
TEON	Tearing Effect Line On/Off	"1" = On, "0" = Off
TELOM	Tearing effect line mode	"0" = mode1, "1" = mode2
HSON	Horizontal Sync. (RGB I/F) On/Off	"1" = On, "0" = Off
VSON	Vertical Sync. (RGB I/F) On/Off	"1" = On, "0" = Off
PCKON	Pixel Clock (PCLK, RGB I/F) On/Off	"1" = On, "0" = Off
DEON	Data Enable (DE, RGB I/F) On/Off	"1" = On, "0" = Off
D1	Not Used	"1" = On, "0" = Off
D0	Not Used	"1" = On, "0" = Off

Restriction

-

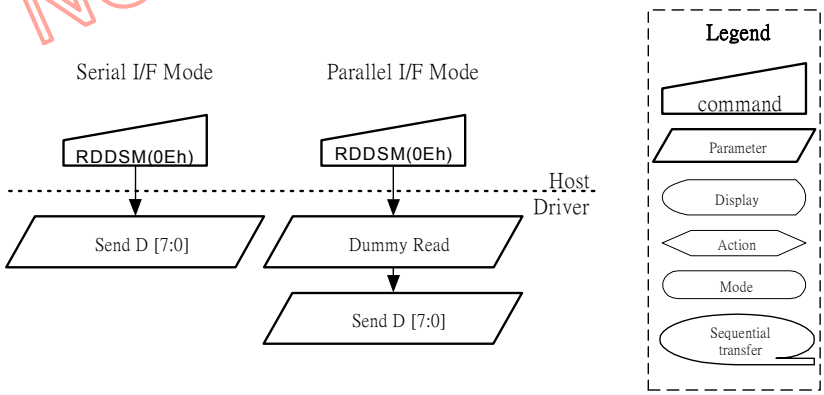
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h (0000_0000)
S/W Reset	00h (0000_0000)

Flow Chart



6.1.10 RDDSDR (0Fh): Read Display Self-Diagnostic Result

0FH	RDDSD (Read Display Self-Diagnostic Result)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDSDR	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	RELD	FUND	ATTD	BRD	D3	D2	D1	D0	00h

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
RELD	Register Loading Detection	See section 5.9.1
FUND	Functionality Detection	See section 5.9.2
ATTD	Chip Attachment Detection	See section 5.9.3
BRD	Display Glass Break Detection	See section 5.9.4
D3	Not Used	"0"
D2	Not Used	"0"
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

-

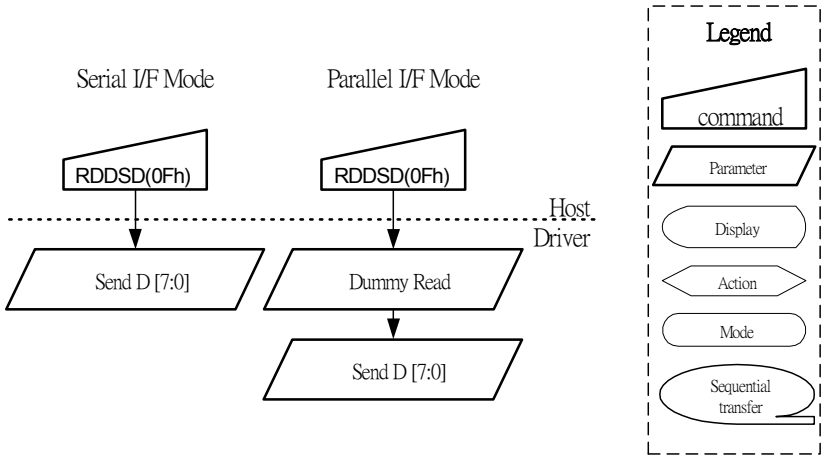
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h (0000_0000)
S/W Reset	00h (0000_0000)

Flow Chart



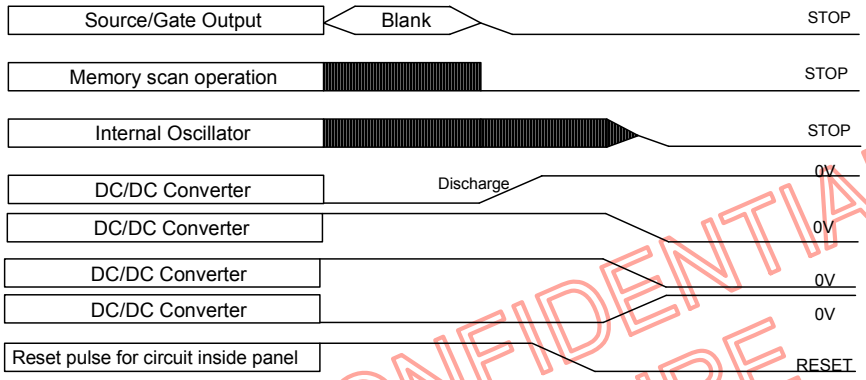
6.1.11 SLPIN (10h): Sleep In

10H	SLPIN (Sleep In)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)
1st parameter	No Parameter												-

NOTE: "-" Don't care

Description

-This command causes the LCD module to enter the minimum power consumption mode.
-In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.



-MPU interface and memory are still working and the memory keeps its contents.

Restriction

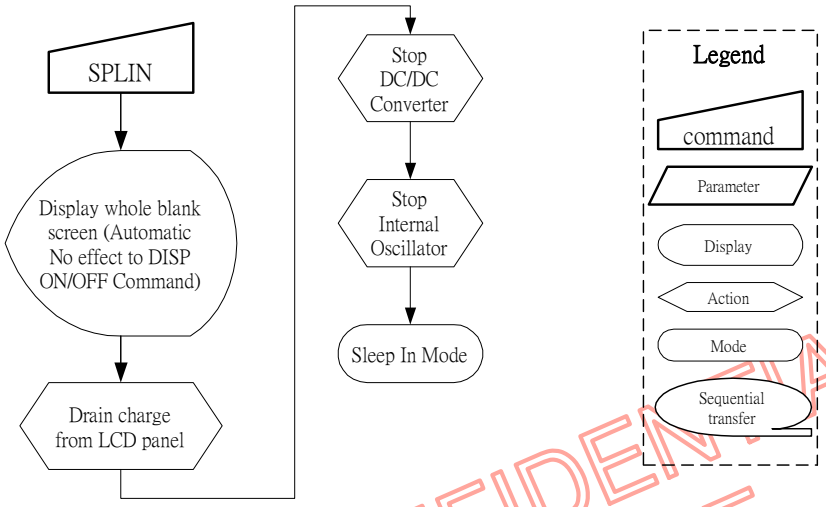
-This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11h).
-It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.
-It will be necessary to wait *120msec* after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode

Flow Chart	-It takes about 120 msec to get into Sleep In mode (booster off state) after SLPIN command issued. -The results of booster off can be check by RDDST (09h) command Bit31. 

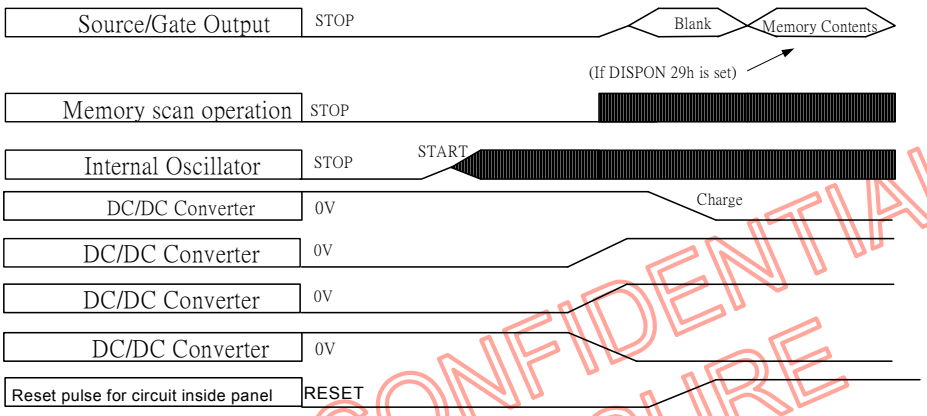
6.1.12 SLPOUT (11h): Sleep Out

11H	SLPOUT (Sleep Out)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)
1st parameter	No Parameter												-

NOTE: "-" Don't care

Description

This command turns off sleep mode.
In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.



Restriction

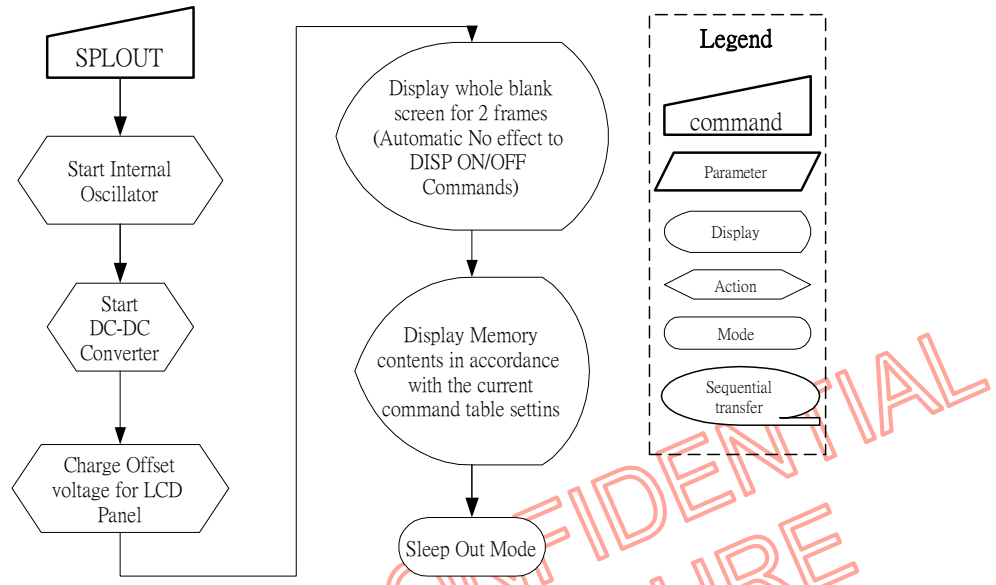
This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10h).
It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.
NT3916 loads all default values of extended and test command to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if those default and register values are same when this load is done and when the NT3916 is already Sleep Out –mode.
NT3916 is doing self-diagnostic functions during this 5msec. See also section 5.14. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

Flow Chart	It takes 120msec to become Sleep Out mode (booster on mode) after SLPOUT command issued. The results of booster on can be checked by RDDST (09h) command Bit31. 

6.1.13 PTLON (12h): Partial Display Mode On

12H	PTLON (Partial Display Mode On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PTLON	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)
1st parameter	No Parameter												-

NOTE: "-" Don't care

Description	-This command turns on Partial mode. The partial mode window is described by the Partial Area command (30H) -To leave Partial mode, the Normal Display Mode On command (13H) should be written. -There is no abnormal visual effect during mode change between Normal mode On <-> Partial mode On.
Restriction	-This command has no effect when Partial mode is active.
Register Availability	Status: Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status: Default Value Power On Sequence: Normal Mode On S/W Reset: Normal Mode On H/W Reset: Normal Mode On
Flow Chart	See Partial Area (30h)

6.1.14 NORON (13h): Normal Display Mode On

13H	NORON (Normal Display Mode On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)
1st parameter	No Parameter												-

NOTE: "-" Don't care

Description	-This command returns the display to normal mode. -Normal display mode on means Partial mode off, Scroll mode Off. -Exit from NORON by the Partial mode On command (12h) -There is no abnormal visual effect during mode change from Normal mode On to Partial mode On.
Restriction	-This command has no effect when Normal Display mode is active.
Register Availability	Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes
Default	Status: Power On Sequence — Default Value: Normal Mode On Status: S/W Reset — Default Value: Normal Mode On Status: H/W Reset — Default Value: Normal Mode On
Flow Chart	-See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command

6.1.15 INVOFF (20h): Display Inversion Off

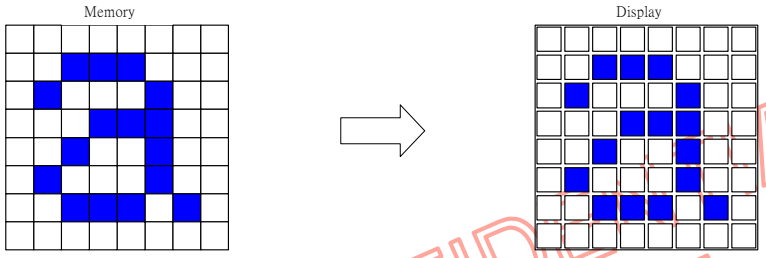
20H	INVOFF (Display Inversion Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)
1st parameter	No Parameter												-

NOTE: "-" Don't care

Description

This command is used to recover from display inversion mode.
This command makes no change of contents of frame memory.
This command does not change any other status.

(Example)



Restriction

This command has no effect when module is already inversion off mode.

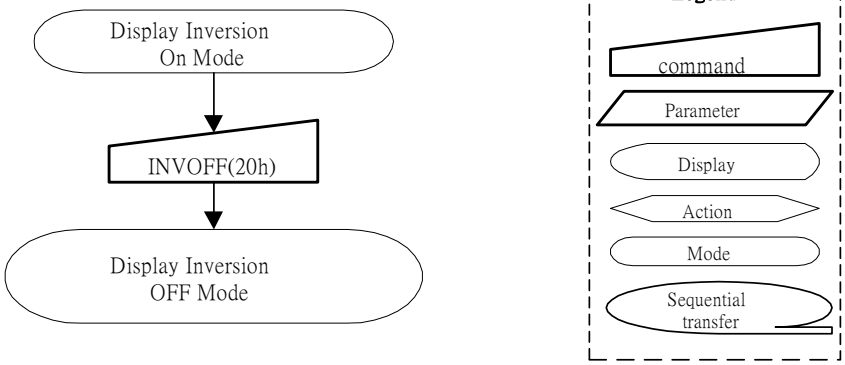
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

Flow Chart



6.1.16 INVON (21h): Display Inversion On

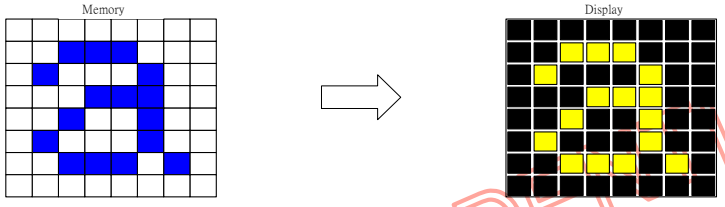
21H	INVON (Display Inversion On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)
1st parameter	No Parameter												-

NOTE: "-" Don't care

Description

This command is used to enter into display inversion mode
This command makes no change of contents of frame memory.
This command does not change any other status.
To exit from Display Inversion On, the Display Inversion Off command (20h) should be written.

(Example)



Restriction

This command has no effect when module is already Inversion On mode.

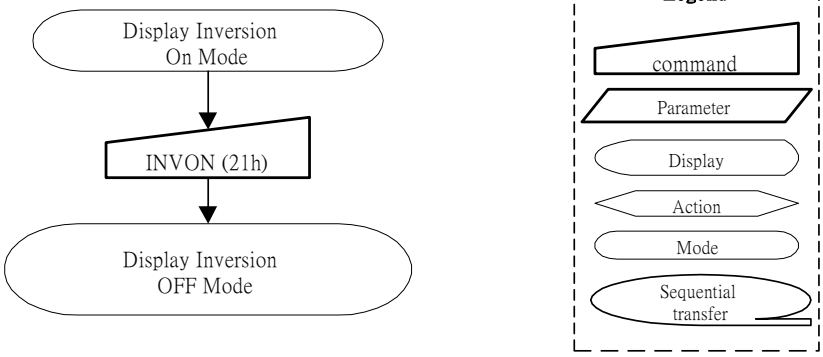
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

Flow Chart



6.1.17 GAMSET (26h): Gamma Set

26H	GAMSET (Gamma Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GAMSET	0	↑	1	-	0	0	1	0	0	1	0	1	(26h)
1st parameter	1	↑	1	-	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	01h

NOTE: "-" Don't care

Description

-This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curves are defined in section 5.5The curve is selected by setting the appropriate bit in the parameter as described in the Table.

GC[7:0]	Parameter	Curve Selected
01h	GC0	Gamma .2.2
02h	GC1	Gamma 1.8
04h	GC2	Gamma 2.5
08h	GC3	Gamma 1.0

Note: All other values are undefined.

Restriction

-Values of GC [7:0] not shown in table above are invalid and will not change the current selected Gamma curve until valid is received.

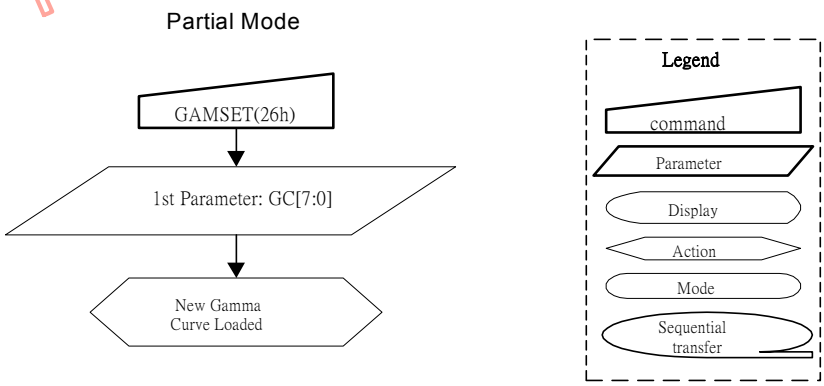
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

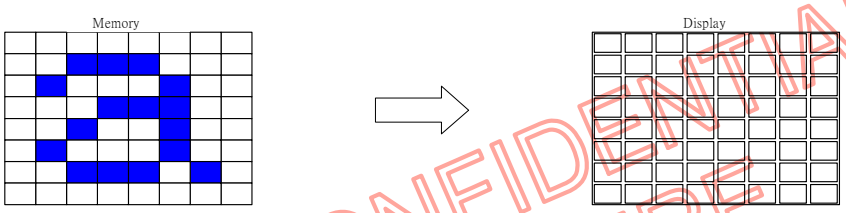
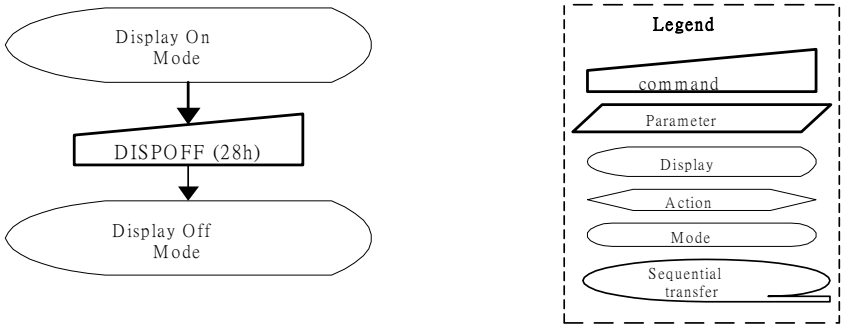
Flow Chart



6.1.18 DISPOFF (28h): Display Off

28H	DISPOFF (Display Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)
1st parameter	No Parameter												-

NOTE: "-" Don't care

Description	-This command is used to enter into DISPLAY OFF mode. In this mode, the output from -Frame Memory is disables and blank page inserted. -This command makes no change of contents of frame memory. -This command does not change any other status. -There will be no abnormal visible effect on the display. -Exit from this command by Display On (29h) (Example) 
Restriction	This command has no effect when module is already in Display Off mode.
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status / Default Value Power On Sequence: Display off S/W Reset: Display off H/W Reset: Display off
Flow Chart	

6.1.19 DISPON (29h): Display On

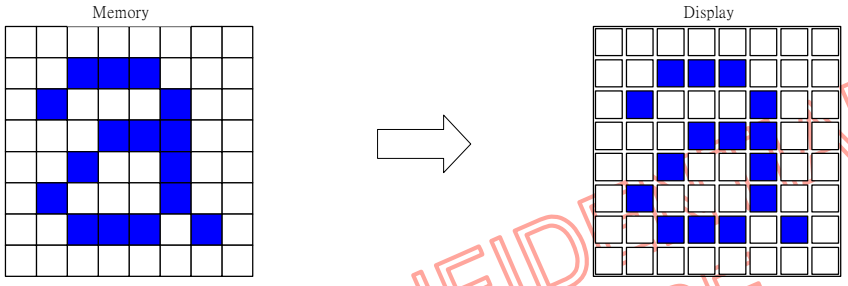
29H	DISPON (Display On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)
1st parameter	No Parameter												-

NOTE: "-" Don't care

Description

-This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.
-This command makes no change of contents of frame memory.
-This command does not change any other status.

(Example)



Restriction

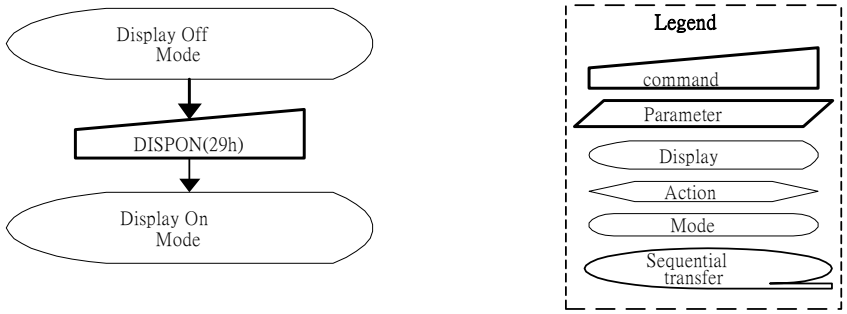
-This command has no effect when module is already in Display On mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart	

6.1.20 CASET (2Ah): Column Address Set

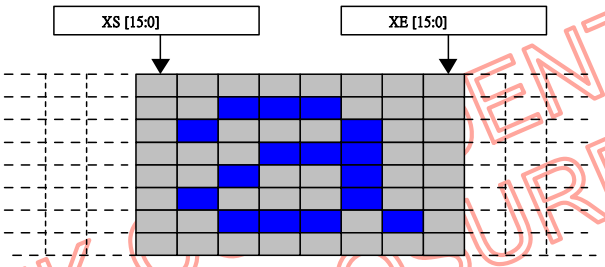
2Ah	CASET (Column Address Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
CASET	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)
1st Parameter	1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	-
2nd Parameter	1	↑	1	-	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	-
3rd Parameter	1	↑	1	-	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	-
4th Parameter	1	↑	1	-	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	-

NOTE: "-" Don't care

Description

-This command is used to define area of frame memory where MPU can access.
-This command makes no change on the other driver status.
-The value of XS [15:0] and XE [15:0] are referred when RAMWR command comes.
-Each value represents one column line in the Frame Memory.

(Example)



Restriction

XS [15:0] always must be equal to or less than XE [15:0]
When XS [15:0] or XE [15:0] is greater than maximum address like below, data of out of range will be ignored.

1. 176X220 memory base (GM='00')
(Parameter range: 0<XS[15:0]< XE[15:0]<175) , MV="0"
(Parameter range: 0<XS[15:0]< XE[15:0]<219) , MV="1"

2. 176X176 memory base (GM='01')
(Parameter range: 0<XS[15:0]< XE[15:0]<175) , MV="0"
(Parameter range: 0<XS[15:0]< XE[15:0]<175) , MV="1"

3. 176X132 memory base (GM='11')
(Parameter range: 0<XS[15:0]< XE[15:0]<175) , MV="0"
(Parameter range: 0<XS[15:0]< XE[15:0]<131) , MV="1"

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

1. 176X220 memory base (GM='00')

Status	Default Value		
	XS [15:0]	XE [15:0] (MV=0)	XE [15:0] (MV=1)
Power On Sequence	0000h	00AFh (175d)	
S/W Reset	0000h	00AFh (175d)	00DBh (219d)
H/W Reset	0000h	00AFh (175d)	

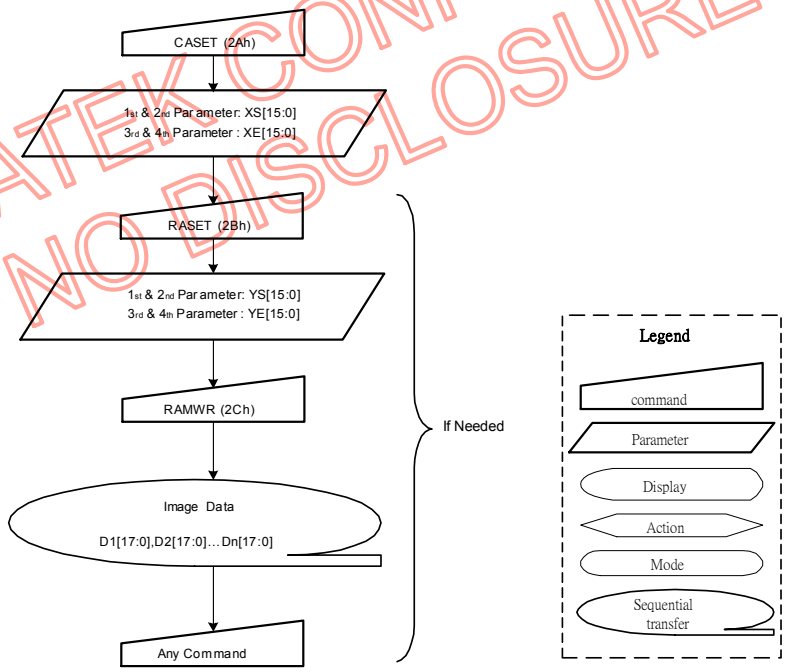
2. 176X176 memory base (GM='01')

Status	Default Value		
	XS [15:0]	XE [15:0] (MV=0)	XE [15:0] (MV=1)
Power On Sequence	0000h	00AFh (175d)	
S/W Reset	0000h	00AFh (175d)	00AFh (175d)
H/W Reset	0000h	00AFh (175d)	

3. 176X132 memory base (GM='11')

Status	Default Value		
	XS [15:0]	XE [15:0] (MV=0)	XE [15:0] (MV=1)
Power On Sequence	0000h	00AFh (175d)	
S/W Reset	0000h	00AFh (175d)	0083h (131d)
H/W Reset	0000h	00AFh (175d)	

Flow Chart



6.1.21 RASET (2Bh): Row Address Set

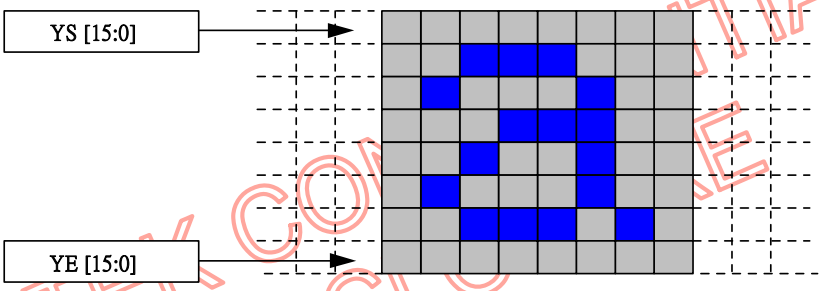
2Bh	RASET (Row Address Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RASET	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)
1st Parameter	1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	-
2nd Parameter	1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	-
3rd Parameter	1	↑	1	-	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	-
4th Parameter	1	↑	1	-	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	-

NOTE: "-" Don't care

Description

-This command is used to define area of frame memory where MPU can access.
-This command makes no change on the other driver status.
-The value of YS [15:0] and YE [15:0] are referred when RAMWR command comes.
-Each value represents one column line in the Frame Memory.

(Example)



Restriction

YS [15:0] always must be equal to or less than YE [15:0]
When YS [15:0] or YE [15:0] are greater than maximum row address like below, data of out of range will be ignored.

1. 176X220 memory base (GM='00')
(Parameter range: 0<YS[15:0]< YE[15:0]<219) , MV="0"
(Parameter range: 0<YS[15:0]< YE[15:0]<175) , MV="1"

2. 176X176 memory base (GM='01')
(Parameter range: 0<YS[15:0]< YE[15:0]<175) , MV="0"
(Parameter range: 0<YS[15:0]< YE[15:0]<175) , MV="1"

3. 176X132 memory base (GM='11')
(Parameter range: 0<YS[15:0]< YE[15:0]<131) , MV="0"
(Parameter range: 0<YS[15:0]< YE[15:0]<175) , MV="1"

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

1. 176X220 memory base (GM='00')

Status	Default Value		
	YS [15:0]	YE [15:0] (MV=0)	YE [15:0] (MV=1)
Power On Sequence	0000h	00DBh (219d)	
S/W Reset	0000h	00DBh (219d)	00AFh (175d)
H/W Reset	0000h	00DBh (219d)	

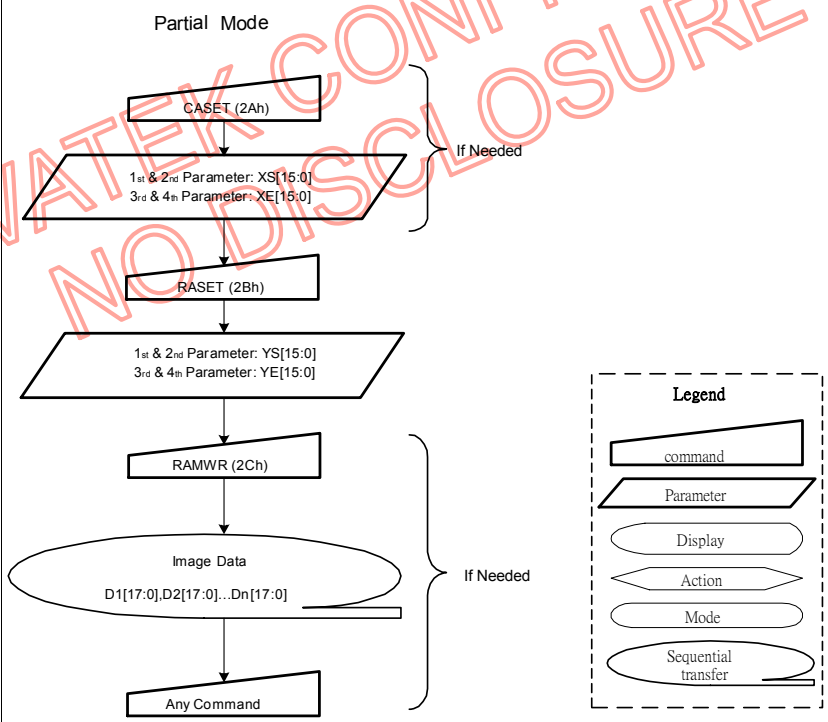
2. 176X176 memory base (GM='01')

Status	Default Value		
	XS [15:0]	XE [15:0] (MV=0)	XE [15:0] (MV=1)
Power On Sequence	0000h	00AFh (175d)	
S/W Reset	0000h	00AFh (175d)	00AFh (175d)
H/W Reset	0000h	00AFh (175d)	

3. 176X132 memory base (GM='11')

Status	Default Value		
	XS [15:0]	XE [15:0] (MV=0)	XE [15:0] (MV=1)
Power On Sequence	0000h	0083h (131d)	
S/W Reset	0000h	0083h (131d)	00AFh (175d)
H/W Reset	0000h	0083h (131d)	

Flow Chart



6.1.22 RAMWR (2Ch): Memory Write

2Ch	RAMWR (Memory Write)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)
1st Parameter	1	↑	1	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-
:	1	↑	1	-	:	:	:	:	:	:	:	:	:
Nth Parameter	1	↑	1	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: "-" Don't care

Description

-This command is used to transfer data MPU to frame memory.
-This command makes no change to the other driver status.
-When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions.
-The Start Column/Start Row positions are different in accordance with MADCTR setting. (See section 5.2.4)
-Then D [17:0] is stored in frame memory and the column register and the row register incremented as section 5.2.4
-Sending any other command can stop Frame Write.

Restriction

In all color modes, there is no restriction on length of parameters.

1. 176X220 memory base (GM='00')
   176x220x18-bit memory can be written by this command
   Memory range: (0000h, 0000h) -> (00AFh, 0DBh)

2. 176X176 memory base (GM='01')
   176x176x18-bit memory can be written by this command
   Memory range: (0000h, 0000h) -> (00AFh, 0AFh)

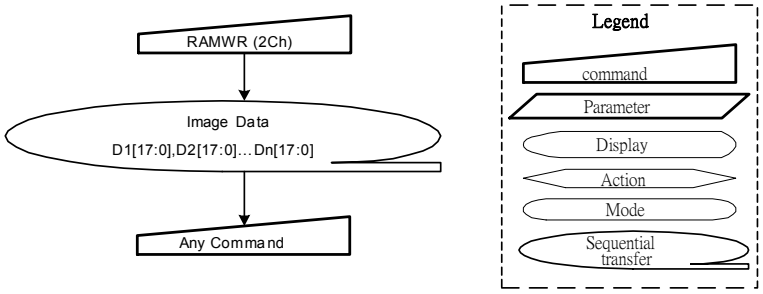
3. 176X132 memory base (GM='11')
   176x132x18-bit memory can be written by this command
   Memory range: (0000h, 0000h) -> (00AFh, 084h)

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart	

6.1.23 RGBSET (2Dh): Color Setting for 4K, 65K and 262K

2Dh	RGBSET (Color Setting for 4K, 65K, and 262K)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RGBSET	0	↑	1	-	0	0	1	0	1	1	0	1	(2Dh)
1st parameter	1	↑	1	-	-	-	R005	R004	R003	R002	R001	R000	-
:	1	↑	1	-	-	-	Rnn5	Rnn4	Rnn3	Rnn2	Rnn1	Rnn0	-
32th parameter	1	↑	1	-	-	-	R315	R314	R313	R312	R311	R310	-
33th parameter	1	↑	1	-	-	-	G005	G004	G003	G002	G001	G000	-
:	1	↑	1	-	-	-	Gnn5	Gnn4	Gnn3	Gnn2	Gnn1	Gnn0	-
96th parameter	1	↑	1	-	-	-	G635	G634	G633	G632	G631	G630	-
97th parameter	1	↑	1	-	-	-	B005	B004	B003	B002	B001	B000	-
:	1	↑	1	-	-	-	Bnn5	Bnn4	Bnn3	Bnn2	Bnn1	Bnn0	-
128th parameter	1	↑	1	-	-	-	B315	B314	B313	B312	B311	B310	-

NOTE: "-" Don't care

Description

This command is used to define the LUT for 12bit-to-18bit / 16-bit -to-18-bit color depth conversations. 128-Bytes must be written to the LUT regardless of the color mode. Only the values in section 5.2.8 are referred.
In this condition, 4K-color (4-4-4), and 65K-color(5-6-5) data input are transferred 6(R)-6(G)-6(B) through RGB LUT table.
This command has no effect on other commands/parameters and Contents of frame memory.
Visible change takes effect next time the Frame Memory is written to.

Restriction

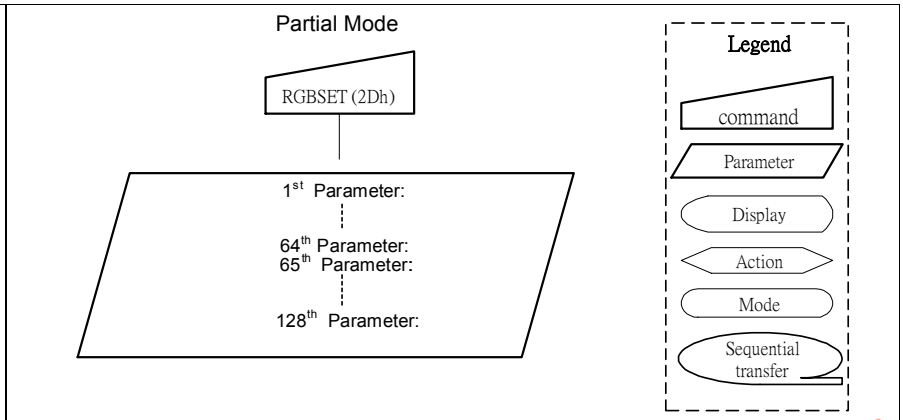
Do not send any command before the last data is sent or LUT is not defined correctly.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	See Section 8.18
S/W Reset	Contents of the look-up table protected
H/W Reset	See Section 8.18

Flow Chart	

6.1.24 RAMRD (2Eh): Memory Read

2Eh	RAMRD (Memory Read)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RAMRD	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	D17	D16	D15	D14	D13	D12	D11	D10	-
:	1	1	↑	-	:	:	:	:	:	:	:	:	:
Nth Parameter	1	1	↑	-	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	-

NOTE: "-" Don't care

Description

-This command is used to transfer data from frame memory to MPU.
-This command makes no change to the other driver status.
-When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions.
-The Start Column/Start Row positions are different in accordance with MADCTR setting. (See section 5.2.4)
-Then D[17:0] is read back from the frame memory and the column register and the row register incremented as section 5.2.4
-Frame Read can be canceled by sending any other command.
-See section 5.2.1 "Display Data Format" for color coding (18 bit cases), when there is used 8, 9, 16 or 18 data lines for image data.

Restriction

In all color modes, the Frame Read is always 24-bit and there is no restriction on length of parameters. Note – Memory Read is only possible via the Parallel Interface.

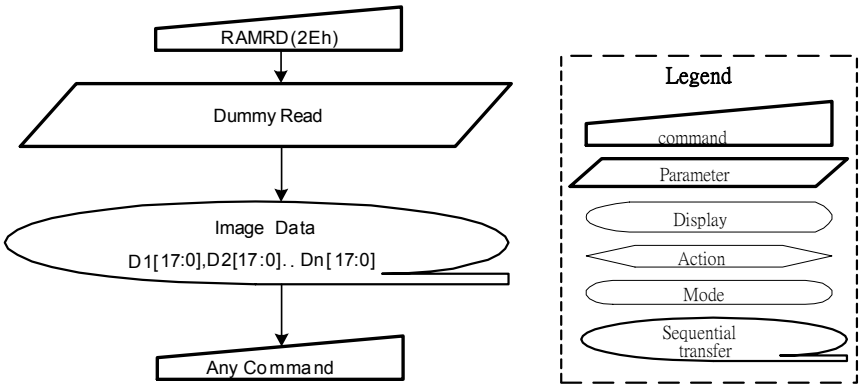
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart



6.1.25 PTLAR (30h): Partial Area

30h	PTLAR (Partial Area)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PTLAR	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)
1st parameter	1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	-
2nd parameter	1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	-
3rd parameter	1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	-
4th parameter	1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	-

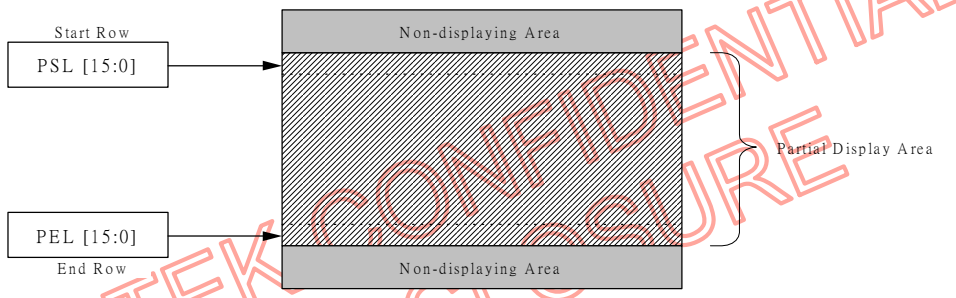
NOTE: "-" Don't care

Description

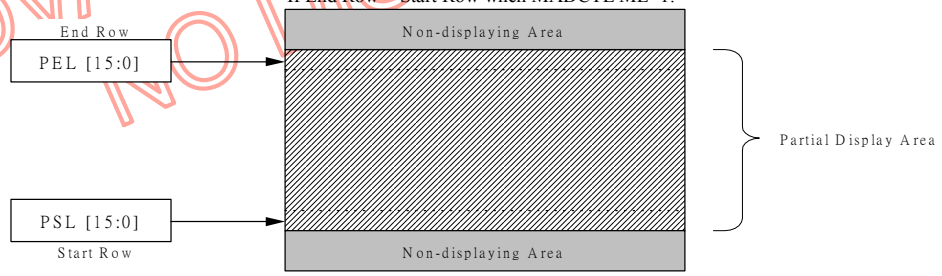
-This command defines the partial mode's display area.

-There are 4 parameters associated with this command, the first defines the Start Row (PSL) and the second the End Row (PEL), as illustrated in the figures below. PSL and PEL refer to the Frame Memory row address counter.

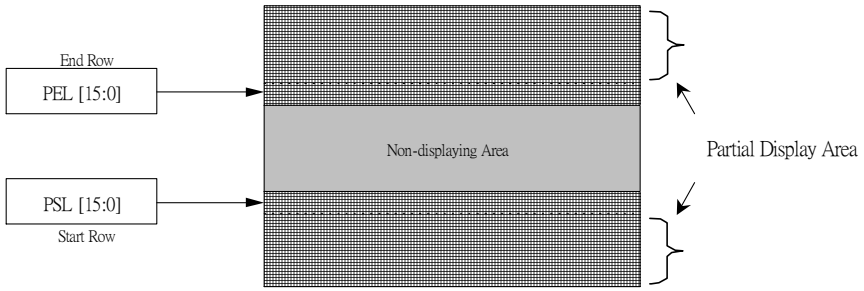
-If End Row > Start Row when MADCTL ML=0:



-If End Row > Start Row when MADCTL ML=1:



-If End Row < Start Row when MADCTL ML=0:



-If End Row = Start Row then the Partial Area will be one row deep.

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

1. 176X220 memory base (GM='00')

Status	Default Value	
	PSL [15:0]	PEL [15:0]
Power On Sequence	0000h	00DBh
S/W Reset		
H/W Reset		

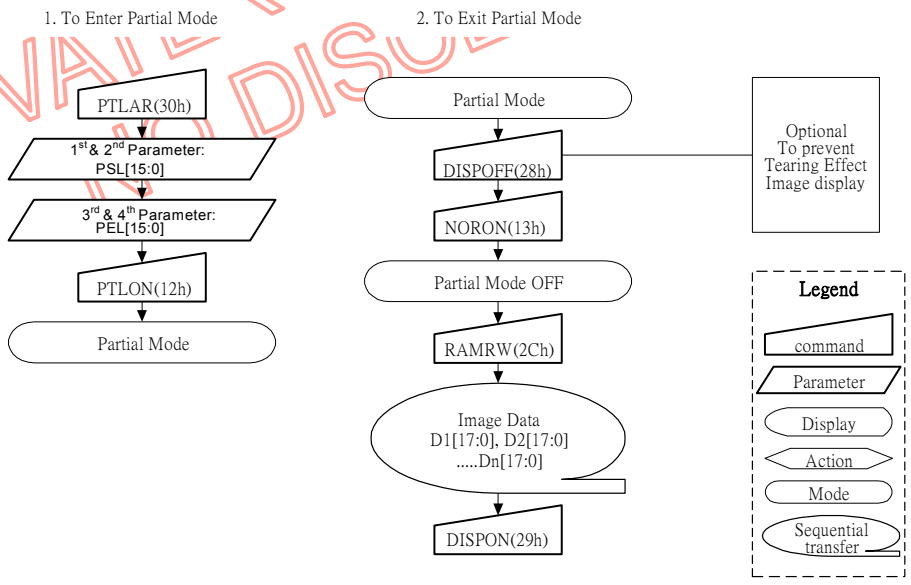
2. 176X176 memory base (GM='01')

Status	Default Value	
	PSL [15:0]	PEL [15:0]
Power On Sequence	0000h	00AFh
S/W Reset		
H/W Reset		

3. 176X132 memory base (GM='11')

Status	Default Value	
	PSL [15:0]	PEL [15:0]
Power On Sequence	0000h	0083h
S/W Reset		
H/W Reset		

Flow Chart



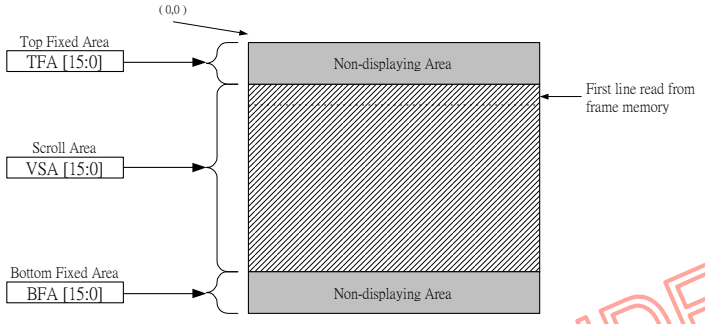
6.1.26 SCRLAR (33h): Scroll Area

33h	SCRLAR (Scroll Area)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SCRLAR	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)
1st parameter	1	↑	1	-	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8	-
2nd parameter	1	↑	1	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	-
3rd parameter	1	↑	1	-	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8	-
4th parameter	1	↑	1	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	-
5th parameter	1	↑	1	-	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8	-
6th parameter	1	↑	1	-	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	-

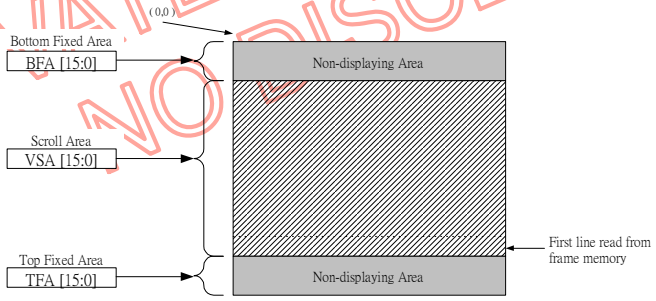
NOTE: "-" Don't care

Description

This command defines the Vertical Scrolling Area of the display.
When MADCTL ML=0
- The 1st & 2nd parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).
- The 3rd & 4th parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address)
- The first line appears immediately after the bottom most line of the Top Fixed Area.
- The 5th & 6th parameter BFA [15:0] describes the Bottom Fixed Area (in No. of lines from TFA, Bottom of the Frame Memory and Display).
- TFA, VSA and BFA refer to the Frame Memory row address



When MADCTL ML=1
- The 1st & 2nd parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).
- The 3rd & 4th parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address)
- The first line appears immediately after the bottom most line of the Top Fixed Area.
- The 5th & 6th parameter BFA [15:0] describes the Bottom Fixed Area (in No. of lines from TFA, Top of the Frame Memory and Display).



See Section5.2.4 for details of the Memory to Display Mapping.

Restriction

The condition is TFA+VSA+BFA=220 in 176RGBx220(GM="00")
The condition is TFA+VSA+BFA=176 in 176RGBx176(GM="01")
The condition is TFA+VSA+BFA=132 in 176RGBx132(GM="11")
-otherwise scrolling mode is undefined.
-In Vertical Scroll Mode, MADCTR parameter MV should be set to '0'-this only affects the Frame Memory Write.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

1. 176X220 memory base (GM='00')

Status	Default Value		
	TFA [15:0]	VSA [15:0]	BFA [15:0]
Power On Sequence	0000h	00DCh	0000h
S/W Reset			
H/W Reset			

2. 176X176 memory base (GM='01')

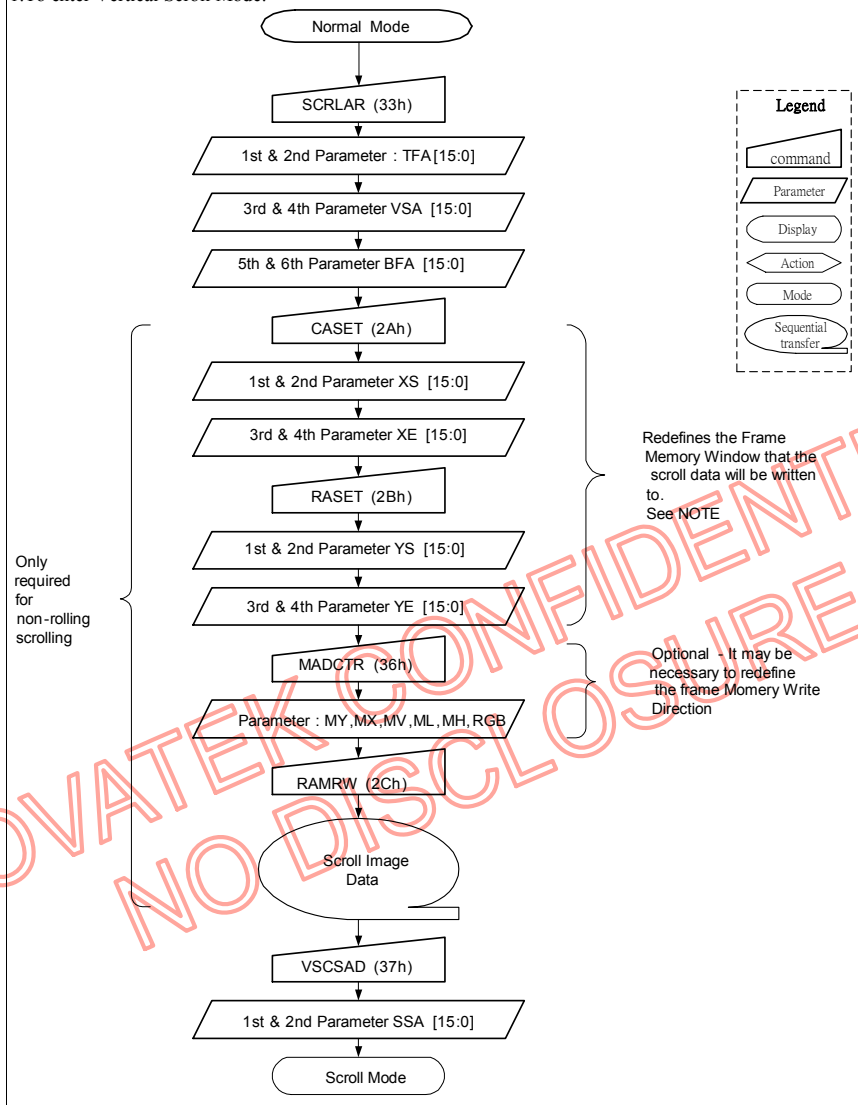
Status	Default Value		
	TFA [15:0]	VSA [15:0]	BFA [15:0]
Power On Sequence	0000h	00B0h	0000h
S/W Reset			
H/W Reset			

3. 176X132 memory base (GM='11')

Status	Default Value		
	TFA [15:0]	VSA [15:0]	BFA [15:0]
Power On Sequence	0000h	0084h	0000h
S/W Reset			
H/W Reset			

Flow Chart

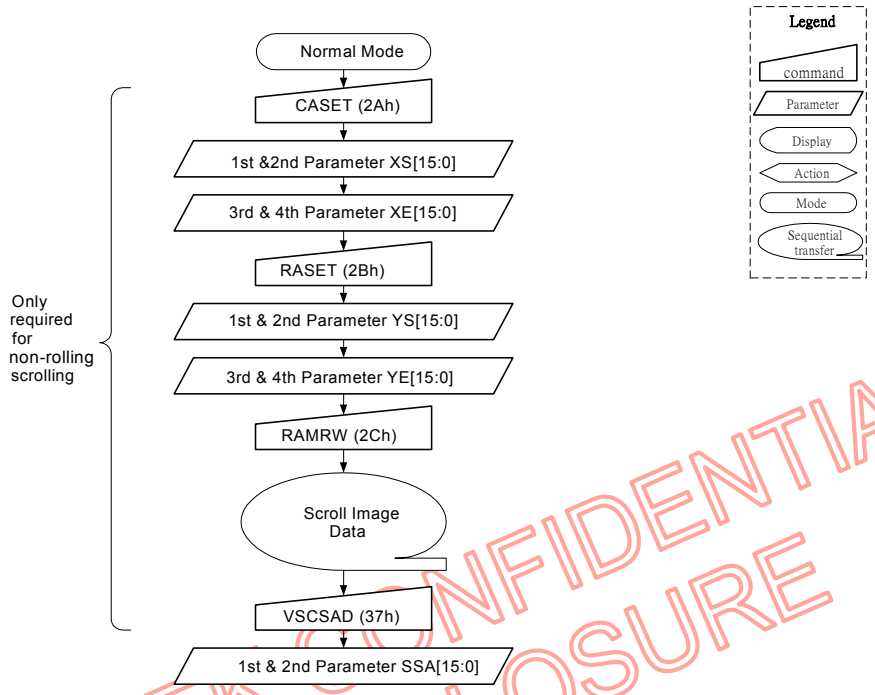
1.To enter Vertical Scroll Mode:



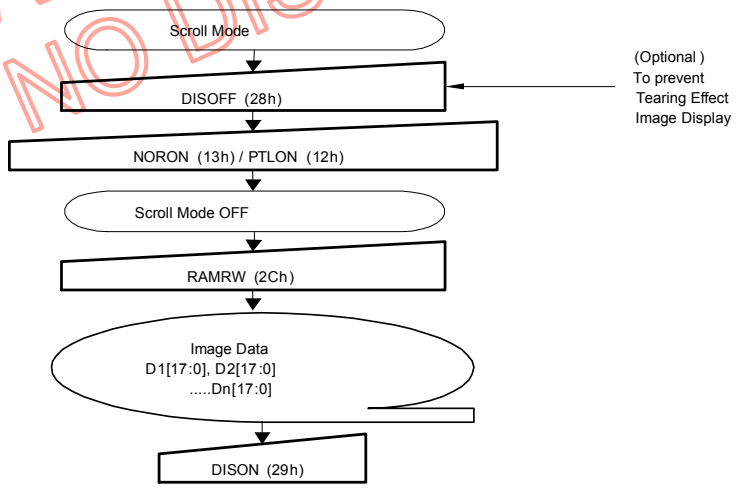
NOTE: The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.

Flow Chart

2. Continuous Scroll:



3. To Exit Vertical Scroll Mode:



NOTE: Scroll Mode can be exit by both the Normal Display Mode On(13h) and Partial Mode On (12h) commands.

6.1.27 TEOFF (34h): Tearing Effect Line OFF

34h	TEOFF (Tearing Effect Line OFF)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)
1st parameter	No Parameter												-

NOTE: "-" Don't care

Description	-This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.
Restriction	-This command has no effect when Tearing Effect output is already OFF.

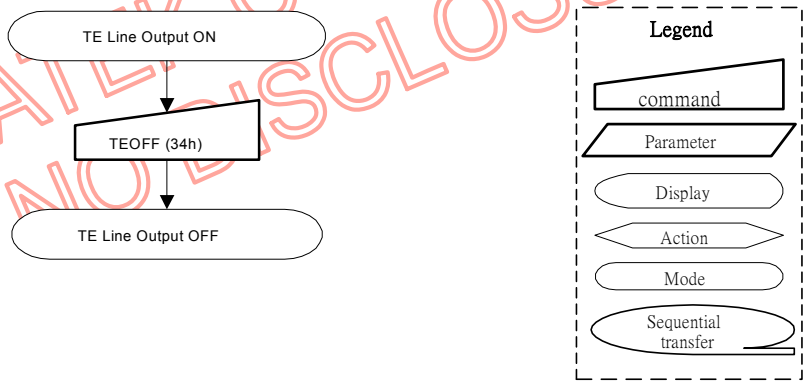
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	RCM="00"	RCM="01"
Power On Sequence	Off	On
S/W Reset	Off	On
H/W Reset	Off	On

Flow Chart



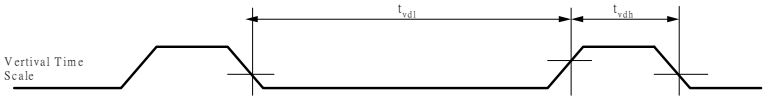
6.1.28 TEON (35h): Tearing Effect Line ON

35h	TEON (Tearing Effect Line ON)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEON	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)
Parameter	1	↑	1	-	-	-	-	-	-	-	-	M	00h

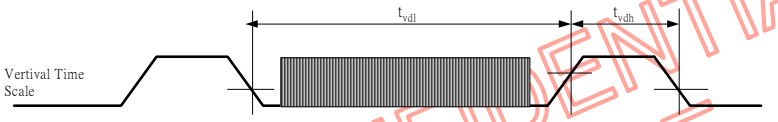
NOTE: "-" Don't care

Description

-This command is used to turn ON the Tearing Effect output signal from the TE signal line.
-This output is not affected by changing MADCTR bit ML.
-The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. ("-"=Don't Care).



—When M='0': The Tearing Effect Output line consists of V-Blanking information only.



—When M='1': The Tearing Effect Output line consists of both V-Blanking and H-Blinking information.

Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

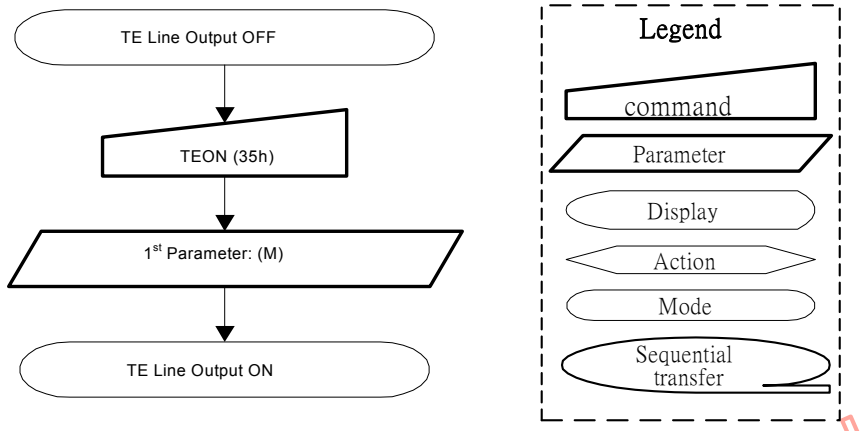
-This command has no effect when Tearing Effect output is already OFF.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	RCM="00"	RCM="01"
Power On Sequence	Off	On (M=0)
S/W Reset	Off	On (M=0)
H/W Reset	Off	On (M=0)

Flow Chart	

6.1.29 MADCTR (36h): Memory Data Access Control

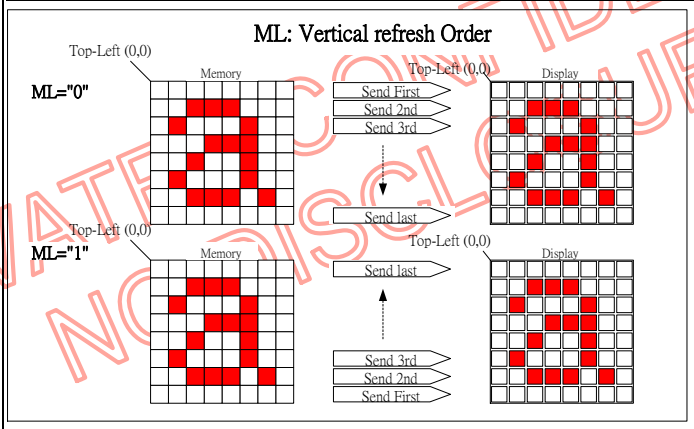
36h	MADCTR (Memory Data Access Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
MADCTL	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)
Parameter	1	↑	1	-	MY	MX	MV	ML	RGB	MH	-	-	00h

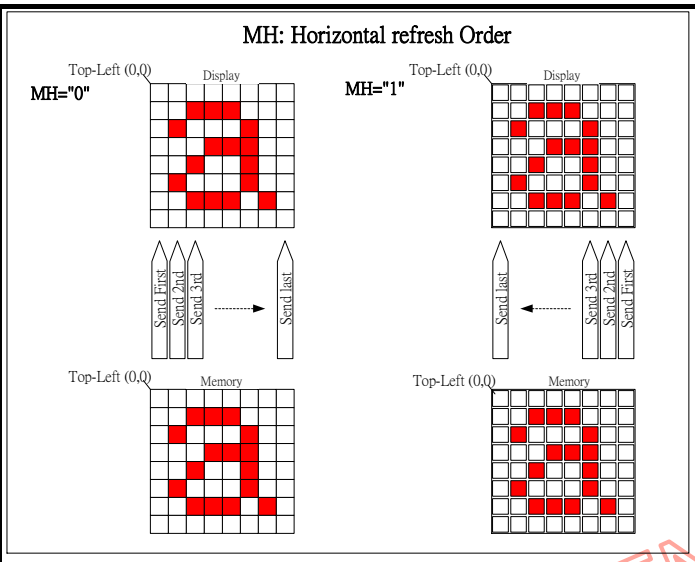
NOTE: "-" Don't care

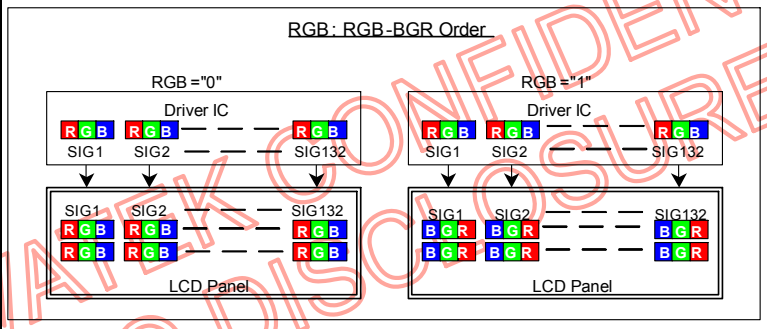
Description

-This command defines read/ write scanning direction of frame memory.
-This command makes no change on the other driver status.
-Bit Assignment

Bit	NAME	DESCRIPTION
MY	ROW ADDRESS ORDER	These 3bits controls MPU to memory write/read direction. (See Section 5.2.3)
MX	COLUMN ADDRESS ORDER	
MV	ROW/COLUMN EXCHANGE	
ML	Vertical refresh ORDER	LCD Vertical refresh direction control
RGB	RGB-BGR ORDER	Color selector switch control 0=RGB color filter panel 1=BGR color filter panel
MH	Display data latch order	'1' =LCD Refresh left to right '0' =LCD Refresh left to right







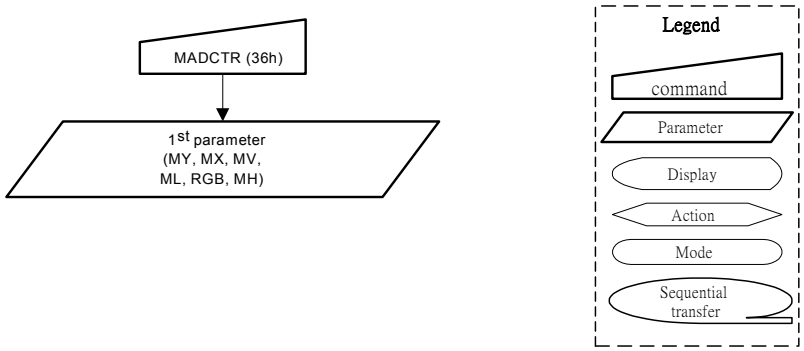
Restriction	-D1 and D0 of the 1st parameter are set to “00” internally.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	No Change
H/W Reset	0000h

Flow Chart	

6.1.30 VSCSAD (37h): Vertical Scroll Start Address of RAM

37h	VSCSAD (Vertical Scroll Start Address of RAM)												
Inst / Para	D/CX	WRX	RDX	**D17-8**	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VSCSAD	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)
1st parameter	1	↑	1	-	SSA15	SSA14	SSA13	SSA12	SSA11	SSA10	SSA9	SSA8	00h
2nd parameter	1	↑	1	-	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	00h

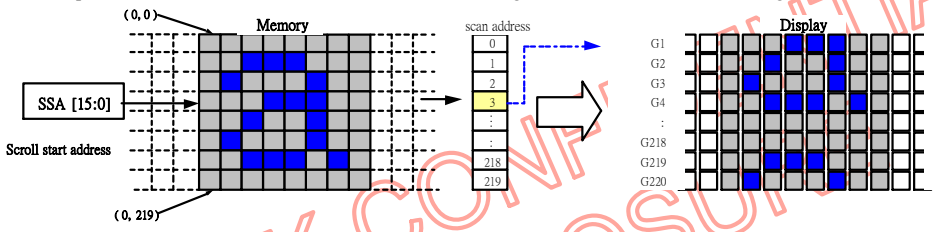
NOTE: "-" Don't care

Description

-This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode.
-The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:
-This command Start the scrolling.

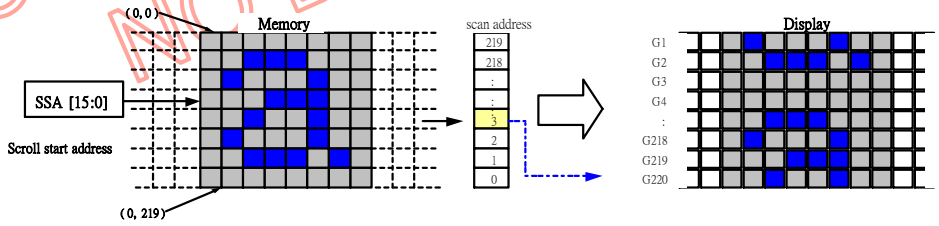
When MADCTL ML=0

Example:
-When Top Fixed Area=Bottom Fixed Area=00, Vertical Scrolling Area=220 and Vertical Scrolling Pointer SSA='3'.



When MADCTL ML =1

Example:
When Top Fixed Area= Bottom Fixed Area=00, Vertical Scrolling Area=220 and SSA='3'



NOTE: -When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.
-SSA refers to the Frame Memory scan address.

Restriction

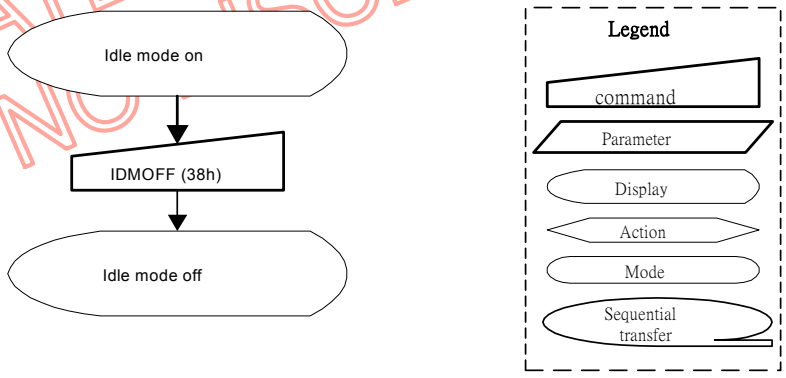
-Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h)-otherwise undesirable image will be displayed on the Panel.
SSA [15:0] is based on 1-line unit.
-SSA [15:0] = 0000h, 0001h, 0002h, 0003h, … , 00DBh

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>0000h</td></tr>
<tr><td>S/W Reset</td><td>0000h</td></tr>
<tr><td>H/W Reset</td><td>0000h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

6.1.31 IDMOFF (38h): Idle Mode Off

38h	IDMOFF (Idle Mode Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)
1st parameter	No Parameter												-

NOTE: "-" Don't care

Description	-This command is used to recover from Idle mode on. -There will be no abnormal visible effect on the display mode change transition. -In the idle off mode, 1. LCD can display maximum 4096,65k, 262k colors. 2. Normal frame frequency is applied.
Restriction	-This command has no effect when module is already in idle off mode.
Register Availability	Status: Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status: Default Value Power On Sequence: Idle Mode Off S/W Reset: Idle Mode Off
Flow Chart	

6.1.32 IDMON (39h): Idle Mode On

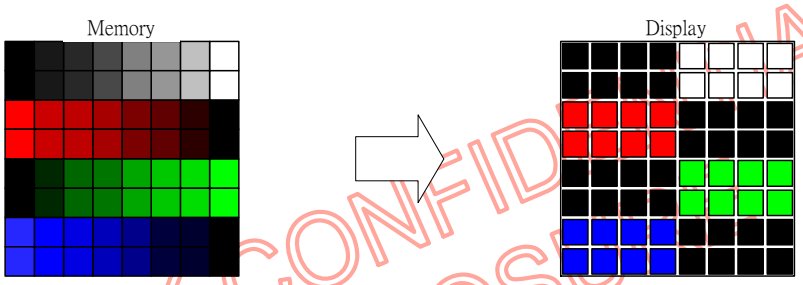
39h	IDMON (Idle Mode On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
IDMON	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)
1st parameter	No Parameter												-

NOTE: "-" Don't care

Description

-This command is used to enter Idle mode on.
-There will be no abnormal visible effect on the display mode change transition.
-In the idle on mode,
1. Color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.
2. 8-Color mode frame frequency is applied.
3. Exit from IDMON by Idle Mode Off (38h) command

(Example)



Color	R5R4R3R2R1R0	G5G4G3G2G1G0	B5B4B3B4B1B0
Black	0XXXXX	0XXXXX	0XXXXX
Blue	0XXXXX	0XXXXX	1XXXXX
Red	1XXXXX	0XXXXX	0XXXXX
Magenta	1XXXXX	0XXXXX	1XXXXX
Green	0XXXXX	1XXXXX	0XXXXX
Cyan	0XXXXX	1XXXXX	1XXXXX
Yellow	1XXXXX	1XXXXX	0XXXXX
White	1XXXXX	1XXXXX	1XXXXX

Restriction

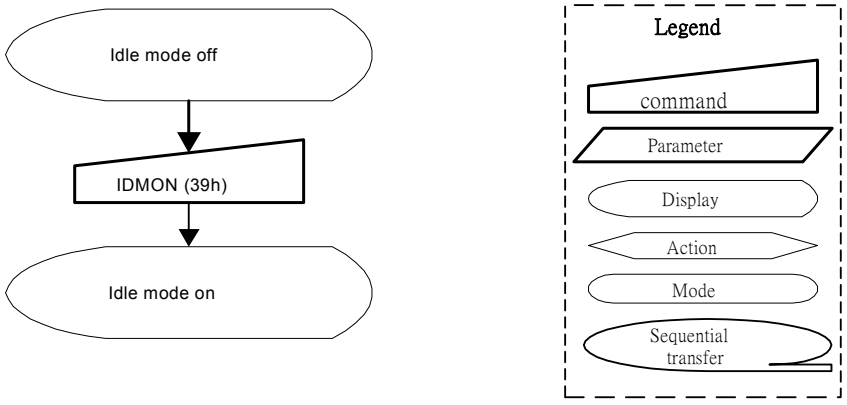
This command has no effect when module is already in idle on mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off

Flow Chart	

6.1.33 COLMOD (3Ah): Interface Pixel Format

3Ah	COLMOD (Interface Pixel Format)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
COLMOD	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)
1st parameter	1	↑	1	-	VIPF3	VIPF2	VIPF1	VIPF0	D3	IFPF2	IFPF1	IFPF0	66h

NOTE: "-" Don't care

Description

This command is used to define the format of RGB picture data, which is to be transferred via the MPU Interface. The formats are shown in the table:

Bit	Description	Value
VIPF3 VIPF2 VIPF1 VIPF0	RGB Interface Color Format	"0101"=16 bit/pixel (1 times data transfer) "0110"=18 bit/pixel (1 times data transfer) "1110"=6 bit/pixel (3 times data transfer) The others = not defined
D3		"0" (Not Used)
IFPF2 IFPF1 IFPF0	Control Interface Color Format	"011"=12 bit/pixel (RGB 4,4,4-bits) "101"=16 bit/pixel (RGB 5,6,5-bits) "110"=18 bit/pixel (RGB 6,6,6-bits) The others = not defined

Note1: In 12-bits/Pixel, 16-bits/Pixel or 18-bits/Pixel mode, the LUT is applied to transfer data into the Frame Memory.
Note2: When RGB I/F the 12-bit/pixel don't care
Note 3: When VIPF[3:0]="1110",6-bits data width of 3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Restriction

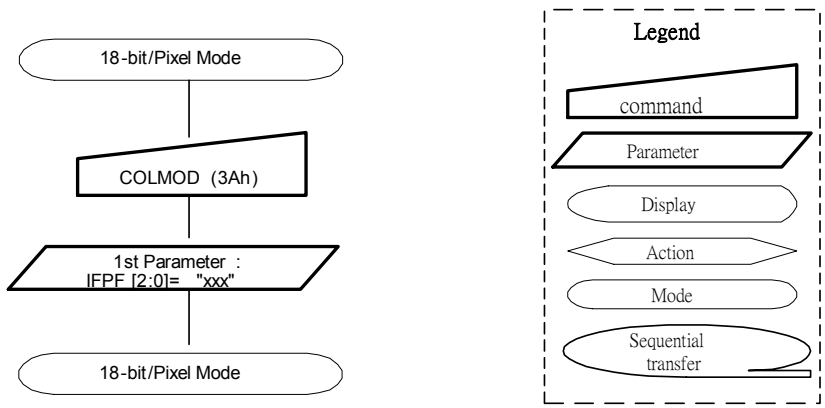
There is no visible effect until the Frame Memory is written to.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	66h (18-Bit/Pixel)
S/W Reset	No Change
H/W Reset	66h (18-Bit/Pixel)

Flow Chart	

6.1.34 RDID1 (DAh): Read ID1 Value

DAh	RDID1 (Read ID1 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	38h

NOTE: "-" Don't care

Description

-This read byte returns 8-bit LCD module's manufacturer ID
-The 1st parameter is dummy data
-The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID.
NOTE: See command RDDID (04h), 2nd parameter.

Restriction

Register Availability

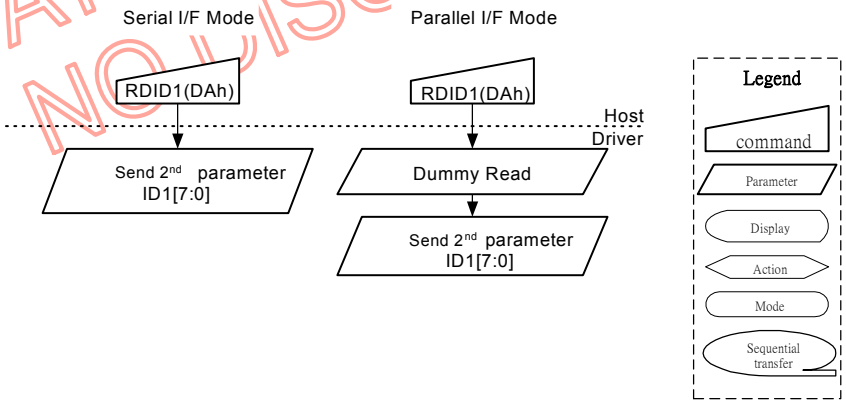
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	38h
S/W Reset	38h
H/W Reset	38h

Note: ID1 can be modified by metal option.

Flow Chart



6.1.35 RDID2 (DBh): Read ID2 Value

DBh	RDID2 (Read ID2 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-

NOTE: "-" Don't care

Description

-This read byte returns 8-bit LCD module/driver version ID
-The 1st parameter is dummy data
-The 2nd parameter (ID26 to ID20): LCD module/driver version ID
-Parameter Range: ID=80h to FFh

D7 to D0	Version	Changes
80h	TBD	TBD
81h	TBD	TBD
82h	TBD	TBD
83h	TBD	TBD
-	TBD	TBD

NOTE: See command RDDID (04h), 3rd parameter.

Restriction

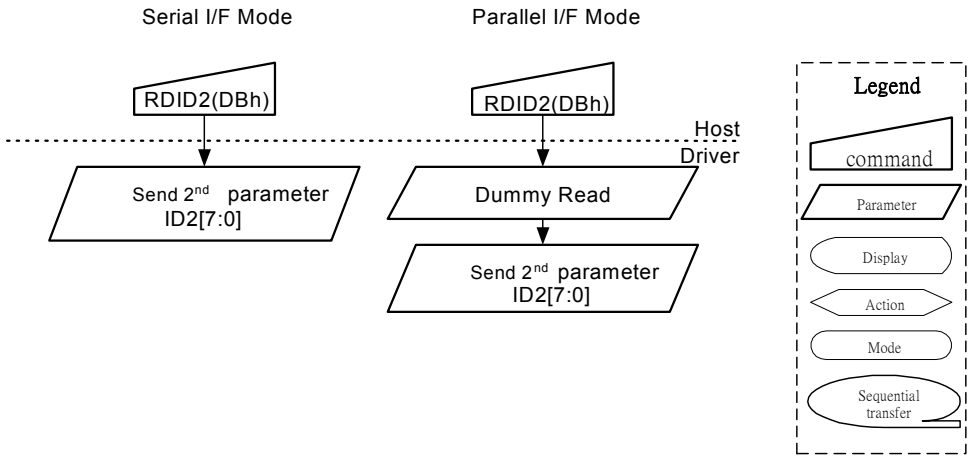
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	MTP value
S/W Reset	MTP value
H/W Reset	MTP value

Flow Chart



6.1.36 RDID3 (DCh): Read ID3 Value

DCh	RDID2 (Read ID2 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DCh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	62h

NOTE: "-" Don't care

Description

-This read byte returns 8-bit LCD module/driver ID
-The 1st parameter is dummy data
-The 2nd parameter (ID37 to ID30): LCD module/driver ID
-Parameter Range: ID=80h to FFh
NOTE: See command RDDID (04h), 4th parameter.

Restriction

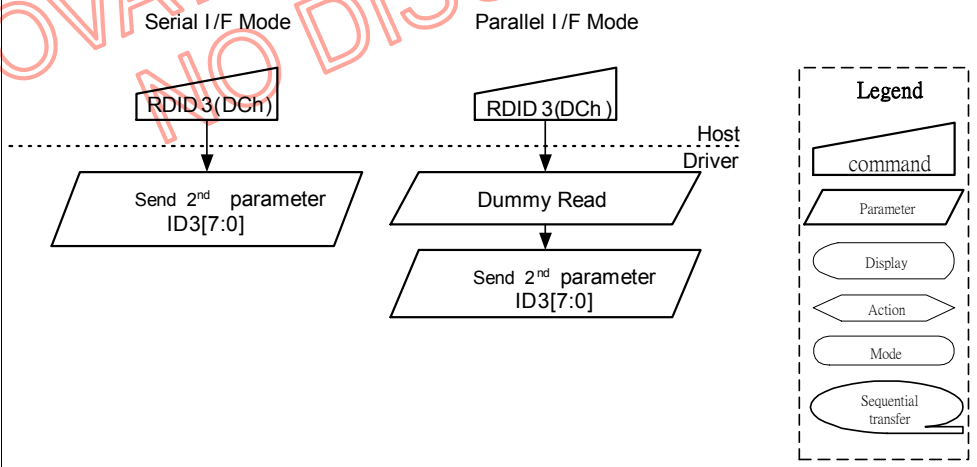
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	MTP value
S/W Reset	MTP value
H/W Reset	MTP value

Flow Chart



6.1.37 SRGBOFF (AAh): Separate RGB Gamma OFF

DCh	SRGBOFF (Separate RGB Gamma OFF)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SRGBOFF	0	↑	1	-	1	0	1	0	1	0	1	0	(AAh)
1st parameter	No Parameter												-

NOTE: "-" Don't care

Description	-This command is used to turn OFF the separate RGB gamma function.
Restriction	-This command has no effect when separate RGB gamma function OFF.

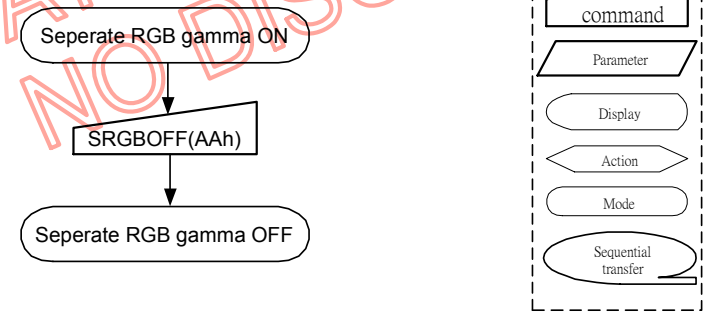
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
S/W Reset	OFF
H/W Reset	OFF

Flow Chart



6.1.38 SRGBON (ABh): Separate RGB Gamma ON

DCh	SRGBON (Separate RGB Gamma ON)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SRGBON	0	↑	1	-	1	0	1	0	1	0	1	1	(ABh)
1st parameter	No Parameter												-

NOTE: "-" Don't care

Description	-This command is used to turn ON the separate RGB gamma function.
Restriction	-This command has no effect when separate RGB gamma function ON.

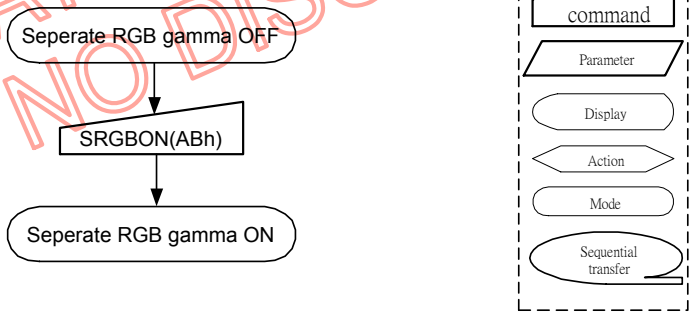
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
S/W Reset	OFF
H/W Reset	OFF

Flow Chart



6.1.39 VSYNCOFF (ACh): VSYNC Interface OFF

DCh	VSYNCOFF (VSYNC Interface OFF)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VSYNCOFF	0	↑	1	-	1	0	1	0	1	1	0	0	(ACh)
1st parameter	No Parameter												-

NOTE: "-" Don't care

Description	-This command is used to turn OFF the VSYNC interface function.
Restriction	-This command has no effect when VSYNC interface OFF. -Input Vs signal foe more than 1 frame period after turn OFF the VSYNC I/F

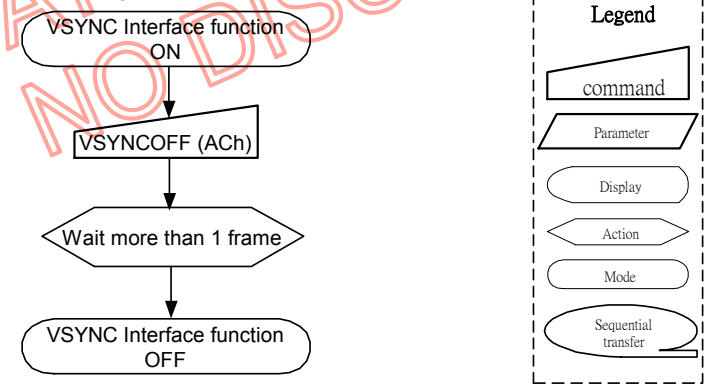
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	RCM="00"	RCM="01"
Power On Sequence	Off	On
S/W Reset	Off	On
H/W Reset	Off	On

Flow Chart



6.1.40 VSYNCON(ADh): VSYNC Interface ON

DCh	VSYNCON (VSYNC Interface ON)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VSYNCON	0	↑	1	-	1	0	1	0	1	1	0	1	(ADh)
1st parameter	No Parameter												-

NOTE: "-" Don't care

Description	-This command is used to turn ON the VSYNC interface function.
Restriction	-This command has no effect when VSYNC interface ON. -Input VS signal before turn On the VSYNC I/F

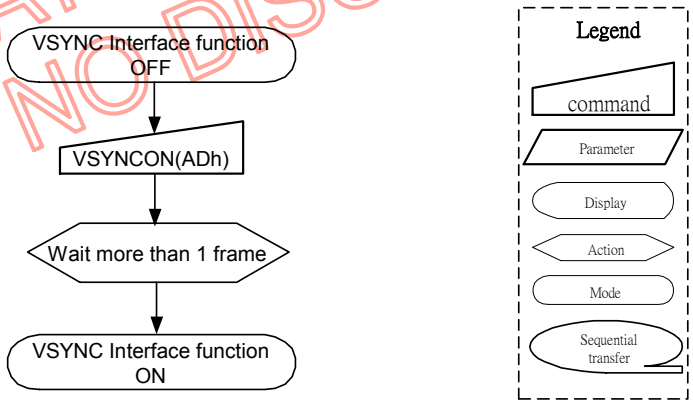
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	RCM="00"	RCM="01"
Power On Sequence	Off	On
S/W Reset	Off	On
H/W Reset	Off	On

Flow Chart



6.1.41 VSCTR1(AEh): VSYNC Interface function control 1

DCh	VSYNCTR1 (VSYNC Interface funtion control 1)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VSCR1	0	↑	1	-	1	0	1	0	1	1	1	0	(AEh)
1st parameter	1	↑	1	-	VSFP3	VSFP2	VSFP1	VSFP0	VSBP3	VSBP2	VSBP1	VSBP0	E2h

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-Set the back porch and front porch on the VSYNC interface. The setting becomes effective as soon as the command is received.

-VSFP: Front porch set on VSYNC I/F

-VSBP: Back porch set on VSYNC I/F

VSFP[3:0] VSBP[3:0]		Front porch period (Line)	Back porch period (Line)
0000	0	Setting inhibited	Setting inhibited
0001	1	Setting inhibited	Setting inhibited
0010	2	**2-lines**	2-lines
0011	3	3-lines	3-lines
0100	4	4-lines	4-lines
0101	5	5-lines	5-lines
0110	6	6-lines	6-lines
0111	7	7-lines	7-lines
1000	8	8-lines	8-lines
1001	9	9-lines	9-lines
1010	10	10-lines	10-lines
1011	11	11-lines	11-lines
1100	12	12-lines	12-lines
1101	13	13-lines	13-lines
1110	14	14-lines	**14-lines**
1111	15	Setting inhibited	Setting inhibited

Restriction

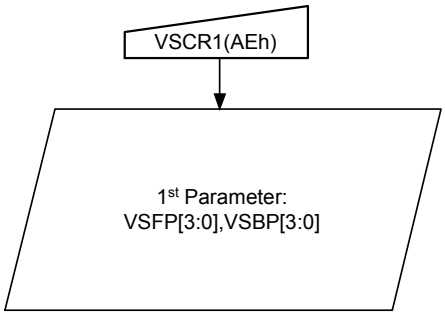
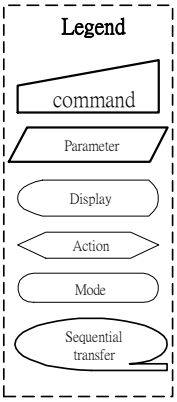
-The command is enabled by VSYNCON (ADh)

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	VSFP[3:0]	VSBP[3:0]
Power On Sequence	02h(2d)	0Eh(14d)
S/W Reset	No change	No change
H/W Reset	02h (2d)	0Eh (14d)

Flow Chart	 

6.2 Panel Function Command List and Description

Table 9.2.1 Panel Function Command List (1)

Instruction	Refer	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
RGBCTR	6.2.1	0	↑	1	-	1	0	1	1	0	0	0	0	(B0h)	Set RGB signal control ICM: RGB data access select DP, HSP, VSP: PCLK, HS, VS polarity set
		1	↑	1	-	0	0	0	ICM	DP	EP	HSP	VSP	-	
					-	0	0	0	0	0	0	0	0		
FRMCTR1	6.2.2	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)	In normal mode (Full colors)
		1	↑	1	-			DIVA5	DIVA4	DIVA3	DIVA2	DIVA1	DIVA0		
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-			VPA5	VPA4	VPA3	VPA2	VPA1	VPA0		
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
FRMCTR2	6.2.3	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)	In Idle mode (8-colors)
		1	↑	1	-			DIVB5	DIVB4	DIVB3	DIVB2	DIVB1	DIVB0		
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-			VPB5	VPB4	VPB3	VPB2	VPB1	VPB0	-	
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
FRMCTR3	6.2.4	0	↑	1	-	1	0	1	1	0	0	1	1	(B3h)	In partial mode + Full colors
		1	↑	1	-			DIVC5	DIVC4	DIVC3	DIVC2	DIVC1	DIVC0		
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-			VPC5	VPC4	VPC3	VPC2	VPC1	VPC0	-	
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
INVCTR	6.2.5	0	↑	1	-	1	0	1	1	0	1	0	0	(B4h)	Display inversion control
		1	↑	1	-	0	0	0	0	0	NLA	NLB	NLC		NLA, NLB, NLC: set inversion
					-	0	0	0	0	0	0	1	0		
RGB PRCTR	6.2.6	0	↑	1	-	1	0	1	1	0	1	0	1	(B5h)	RGB I/F Blanking porch setting
		1	↑	1	-			HBP5	HBP4	HBP3	HBP2	HBP1	HBP0		HS back porch setting
					-	0	0	0	0	0	0	0	0		
		1	↑	1		VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0		VS back porch setting
		1	↑	1								VBP9	VBP8		
DISSET5	6.2.7	0	↑	1	-	1	0	1	1	0	1	1	1	(B6h)	Display function setting
		1	↑	1	-	0	0	NO1	NO0	SDT1	SDT0	EQ1	EQ0		NO: the amount of non-overlap SDT: set amount of source delay PT: No display area source/ VCOM/ Gate output control EQ: set EQ period
					-	0	0	0	1	0	1	1	0		
		1	↑	1	-	0	0	0	0	PTG1	PTG0	PT1	PT0		
					-	0	0	0	0	0	0	1	0		
DISSET6	6.2.8	0	↑	1	-	1	0	1	1	0	1	1	1	(B7h)	SD output direction control
		1	↑	1	-								CRL		
					-	0	0	0	0	0	0	0	0		
DISSET7	6.2.9	0	↑	1	-	1	0	1	1	1	0	0	0	(B8h)	GD output direction control
		1	↑	1	-								CTB		
					-	0	0	0	0	0	0	0	0		
DISSET8		0	↑	1	-	1	0	1	1	1	0	0	1	(B9h)	Reserved for future using
		1	↑	1	-	0	0	0	0	0	0	0	0		
					-	0	0	0	0	0	0	0	0		

"-": Don't care

Note 1: B0h to BFh are fixed for about display function setting

Note 2: B7h to B9h registers are reserved for future using.

Table 6.2.1 Panel Function Command List (2)

Instruction	Refer	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
PWCTR1	6.2.8	0	↑	1	-	1	0	1	1	0	0	0	0	(C0h)	Power control setting
		1	↑	1	-	0	0	0	VRH4	VRH3	VRH2	VRH1	VRH0		VRH: Set the GVDD voltage
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	0	0	0	0	0	VC2	VC1	VC0		VC: Set the VCI1 voltage
					-	0	0	0	0	0	0	1	1		
PWCTR2	6.2.9	0	↑	1	-	1	0	1	1	0	0	0	1	(C1h)	Power control setting
		1	↑	1	-	0	0	0	0	0	BT2	BT1	BT0		BT:set AVDD/VCL/VGH/ VGL voltage
					-	0	0	0	0	0	1	1	1		
PWCTR3	6.2.10	0	↑	1	-	1	0	1	1	0	0	1	0	(C2h)	In normal mode (Full colors)
		1	↑	1	-	0	0	0	0	0	APA2	APA 1	APA 0		AP: adjust the operational amplifier
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	0	0	0	0	0	DCA2	DCA1	DCA0		DC: adjust the booster circuit for Idle mode
					-	0	0	0	0	0	0	0	0		
PWCTR4	6.2.11	0	↑	1	-	1	0	1	1	0	0	1	1	(C3h)	In Idle mode (8-colors)
		1	↑	1	-	0	0	0	0	0	APB2	APB1	APB0		AP: adjust the operational amplifier
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	0	0	0	0	0	DCB2	DCB1	DCB0		DCT: adjust the booster circuit for Idle mode
					-	0	0	0	0	0	0	0	0		
PWCTR5	6.2.12	0	↑	1	-	1	0	1	1	0	1	0	0	(C4h)	In partial mode + Full colors
		1	↑	1	-	0	0	0	0	0	APC2	APC1	APC0		AP: adjust the operational amplifier
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	0	0	0	0	0	DCC2	DCC1	DCC0		DCT: adjust the booster circuit for Idle mode
					-	0	0	0	0	0	0	0	0		
VMCTR1	6.2.13	0	↑	1	-	1	0	1	1	0	1	0	1	(C5h)	VCOM control 1
		1	↑	1	-	-	VMH6	VMH5	VMH4	VMH3	VMH	VMH1	VMH0		VMH:VCOMH voltage control
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	0	VML6	VML5	VML4	VML3	VML2	VML1	VML0		VML: VCOML voltage control
					-	0	0	0	0	0	0	0	0		
VMOF CTR	6.2.15	0	↑	1	-	1	0	1	1	0	1	1	1	(C7h)	VCOM control 3
		1	↑	1	-	nVM	VMF6	VMF5	VMF4	VMF3	VMF2	VMF1	VMF0		VMF: VCOM offset control
					-	0	0	0	0	0	0	0	0		
RVMOF CTR	6.2.16	0	1	↑	-	1	0	1	1	1	0	0	0	(C8h)	VCOM control 4
		1	1	↑	-		RVMF6	RVMF5	RVMF4	RVMF3	RVMF2	RVMF1	RVMF0	-	Read the VMOF value form NV memory
					-	0	0	0	0	0	0	0	0	-	
PWCTR6		0	↑	1	-	1	0	1	1	1	0	0	1	(C9h)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
PWCTR7		0	↑	1	-	1	0	1	1	1	0	1	0	(CAh)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
PWCTR8		0	↑	1	-	1	0	1	1	1	0	1	1	(CBh)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Reserved		0	↑	1	-	1	0	1	1	1	1	0	0	(CCh)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Reserved		0	↑	1	-	1	0	1	1	1	1	0	1	(CDh)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Reserved		0	↑	1	-	1	0	1	1	1	1	1	0	(CEh)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Reserved		0	↑	1	-	1	0	1	1	1	1	1	1	(CFh)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		

"-": Don't care

Note 1: C0h to CFh are fixed for about power controller.

Note 2: The C9h to CFh are reserved for further using.

Table 6.2.1 Panel Function Command List (3)

Instruction	Refer	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
ID1		0	↑	1	-	1	1	0	1	0	0	0	0	(D0h)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
WRID2	6.2.18	0	↑	1	-	1	1	0	1	0	0	0	1	(D1h)	LCM version code
		1	↑	1	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20		Write ID2 value to NV memory Set the LCM version code at ID2
					-	0	0	0	0	0	0	0	0		
WRID3	6.2.19	0	↑	1	-	1	1	0	1	0	0	1	0	(D2h)	Customer Project code
		1	↑	1	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		Write ID3 value to NV memory Set the project code at ID3
					-	0	0	0	0	0	0	0	0		
RDID4	6.2.20	0	↑	1	-	1	1	0	1	0	0	1	1	(D3h)	IC Vender Coder
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
					-	-	-	-	-	-	-	-	-		
		1	1	↑	-	ID417	ID416	ID415	ID414	ID413	ID412	ID411	ID410		ID41:IC Vender Coder ID42: IC Part Number Coder ID43 & ID44: Chip version coder
					-	0	0	0	0	0	0	0	0		
		1	1	↑	-	ID427	ID426	ID425	ID424	ID423	ID422	ID421	ID420		
					-	0	0	0	0	0	0	0	0		
		1	1	↑	-	-	-	-	-	ID433	ID432	ID431	ID430		
					-	-	-	-	-	0	0	0	0		
ID5		0	↑	1	-	1	1	0	1	0	1	0	0	(D4h)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
ID6		0	↑	1	-	1	1	0	1	0	1	0	1	(D5h)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
ID7		0	↑	1	-	1	1	0	1	0	1	1	0	(D6h)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
ID8		0	↑	1	-	1	1	0	1	0	1	1	1	(D7h)	Reserved for future using
		1	↑	1											
					-										
Reserved		0	↑	1	-	1	1	0	1	1	1	0	0	(D8h)	Reserved for future using
		1	↑	1											
					-										
NVCTR1	6.2.21	0	↑	1	-	1	1	0	1	1	1	0	1	(D9h)	NV memory function controller 1
		1	↑	1	-								EP_PWR	-	
					-	0	0	0	0	0	0	0	0		
EPWRITE	6.2.22	0	↑	1	-	1	1	0	1	1	1	1	0	(DEh)	MTP write command
EPCLR	6.2.23	0	↑	1	-	1	1	0	1	1	1	1	1	(DFh)	MTP read command

"-": Don't care

Note 1: The D0h to D8h registers are fixed for about ID code setting.

Note 2: The D9h, DEh and DFh registers are used for NV Memory function controller. (Ex: write, clear, etc.) Note 3: The D4h to D8h registers are reserved for future using.

Table 6.2.1 Panel Function Command List (4)

Instruction	Refer	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
GAMCTRP1	6.2.27	0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)	Set Gamma correction
		1	↑	1	-	-	PKP12	PKP11	PKP10	-	PKP02	PKP01	PKP00	-	Gamma adjustment (+ polarity)
		1	↑	1	-	-	PKP32	PKP31	PKP30	-	PKP22	PKP21	PKP20		
		1	↑	1	-	-	PKP52	PKP51	PKP50	-	PKP42	PKP41	PKP40		
		1	↑	1	-	-	-	-	PRP04	PRP03	PRP02	PRP01	PRP00		
		1	↑	1	-	PRP23	PRP22	PRP21	PRP20	PRP13	PRP12	PRP11	PRP10		
		1	↑	1	-	-	-	-	-	PRP33	PRP32	PRP31	PRP30		
		1	↑	1	-	-	-	-	PRP44	PRP43	PRP42	PRP41	PRP40		
		1	↑	1	-	VRP13	VRP12	VRP11	VRP10	VRP03	VRP02	VRP01	VRP00		
GAMCTRN1	6.2.28	0	↑	1	-	1	1	1	0	0	0	0	1	(E1h)	Set Gamma correction
		1	↑	1	-	-	PKN12	PKN11	PKN10	-	PKN02	PKN01	PKN00	-	Gamma adjustment (- polarity)
		1	↑	1	-	-	PKN32	PKN31	PKN30	-	PKN22	PKN21	PKN20		
		1	↑	1	-	-	PKN52	PKN51	PKN50	-	PKN42	PKN41	PKN40		
		1	↑	1	-	-	-	-	PRN04	PRN03	PRN02	PRN01	PRN00		
		1	↑	1	-	PRN23	PRN22	PRN21	PRN20	PRN13	PRN12	PRN11	PRN10		
		1	↑	1	-	-	-	-	-	PRN33	PRN32	PRN31	PRN30		
		1	↑	1	-	-	-	-	PRN44	PRN43	PRN42	PRN41	PRN40		
		1	↑	1	-	VRN13	VRN12	VRN11	VRN10	VRN03	VRN02	VRN01	VRN00		
GAMCTRP2	6.2.29	0	↑	1	-	1	1	1	0	0	0	1	0	(E2h)	Set Gamma correction
		1	↑	1	-	-	PKN12	PKN11	PKN10	-	PKN02	PKN01	PKN00	-	Gamma adjustment (+ polarity)
		1	↑	1	-	-	PKN32	PKN31	PKN30	-	PKN22	PKN21	PKN20		
		1	↑	1	-	-	PKN52	PKN51	PKN50	-	PKN42	PKN41	PKN40		
		1	↑	1	-	-	-	-	PRN04	PRN03	PRN02	PRN01	PRN00		
		1	↑	1	-	PRN23	PRN22	PRN21	PRN20	PRN13	PRN12	PRN11	PRN10		
		1	↑	1	-	-	-	-	-	PRN33	PRN32	PRN31	PRN30		
		1	↑	1	-	-	-	-	PRN44	PRN43	PRN42	PRN41	PRN40		
		1	↑	1	-	VRN13	VRN12	VRN11	VRN10	VRN03	VRN02	VRN01	VRN00		
GAMCTRN2	6.2.30	0	↑	1	-	1	1	1	0	0	0	1	1	(E3h)	Set Gamma correction
		1	↑	1	-	-	PKN12	PKN11	PKN10	-	PKN02	PKN01	PKN00	-	Gamma adjustment (- polarity)
		1	↑	1	-	-	PKN32	PKN31	PKN30	-	PKN22	PKN21	PKN20		
		1	↑	1	-	-	PKN52	PKN51	PKN50	-	PKN42	PKN41	PKN40		
		1	↑	1	-	-	-	-	PRN04	PRN03	PRN02	PRN01	PRN00		
		1	↑	1	-	PRN23	PRN22	PRN21	PRN20	PRN13	PRN12	PRN11	PRN10		
		1	↑	1	-	-	-	-	-	PRN33	PRN32	PRN31	PRN30		
		1	↑	1	-	-	-	-	PRN44	PRN43	PRN42	PRN41	PRN40		
		1	↑	1	-	VRN13	VRN12	VRN11	VRN10	VRN03	VRN02	VRN01	VRN00		
GAMCTRP3	6.2.31	0	↑	1	-	1	1	1	0	0	1	0	0	(E4h)	Set Gamma correction
		1	↑	1	-	-	PKN12	PKN11	PKN10	-	PKN02	PKN01	PKN00	-	Gamma adjustment (+ polarity)
		1	↑	1	-	-	PKN32	PKN31	PKN30	-	PKN22	PKN21	PKN20		
		1	↑	1	-	-	PKN52	PKN51	PKN50	-	PKN42	PKN41	PKN40		
		1	↑	1	-	-	-	-	PRN04	PRN03	PRN02	PRN01	PRN00		
		1	↑	1	-	PRN23	PRN22	PRN21	PRN20	PRN13	PRN12	PRN11	PRN10		
		1	↑	1	-	-	-	-	-	PRN33	PRN32	PRN31	PRN30		
		1	↑	1	-	-	-	-	PRN44	PRN43	PRN42	PRN41	PRN40		
		1	↑	1	-	VRN13	VRN12	VRN11	VRN10	VRN03	VRN02	VRN01	VRN00		
GAMCTRN3	6.2.32	0	↑	1	-	1	1	1	0	0	1	0	1	(E5h)	Set Gamma correction
		1	↑	1	-	-	PKN12	PKN11	PKN10	-	PKN02	PKN01	PKN00	-	Gamma adjustment (- polarity)
		1	↑	1	-	-	PKN32	PKN31	PKN30	-	PKN22	PKN21	PKN20		
		1	↑	1	-	-	PKN52	PKN51	PKN50	-	PKN42	PKN41	PKN40		
		1	↑	1	-	-	-	-	PRN04	PRN03	PRN02	PRN01	PRN00		
		1	↑	1	-	PRN23	PRN22	PRN21	PRN20	PRN13	PRN12	PRN11	PRN10		
		1	↑	1	-	-	-	-	-	PRN33	PRN32	PRN31	PRN30		
		1	↑	1	-	-	-	-	PRN44	PRN43	PRN42	PRN41	PRN40		
		1	↑	1	-	VRN13	VRN12	VRN11	VRN10	VRN03	VRN02	VRN01	VRN00		
GAMCTR5		0	↑	1	-	1	1	1	0	0	1	1	0	(E6h)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
GAMCTR6		0	↑	1	-	1	1	1	0	0	1	1	1	(E7h)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Reserved		0	↑	1	-	1	1	1	0	1	0	0	0	(E8h)	Reserved for future using

		1	↑	1	-											
					-	0	0	0	0	0	0	0	0			
Reserved		0	↑	1	-	1	1	1	0	1	0	0	1	(E9h)	Reserved for future using	
		1	↑	1	-											
					-	0	0	0	0	0	0	0	0			
Reserved		0	↑	1	-	1	1	1	0	1	0	1	0	(EAh)	Reserved for future using	
		1	↑	1	-											
					-	0	0	0	0	0	0	0	0			
Reserved		0	↑	1	-	1	1	1	0	1	0	1	1	(EBh)	Reserved for future using	
		1	↑	1	-											
					-	0	0	0	0	0	0	0	0			
Reserved		0	↑	1	-	1	1	1	0	1	1	0	0	(ECh)	Reserved for future using	
		1	↑	1	-											
					-	0	0	0	0	0	0	0	0			
Reserved		0	↑	1	-	1	1	1	0	1	1	0	1	(EDh)	Reserved for future using	
		1	↑	1	-											
					-	0	0	0	0	0	0	0	0			
Reserved		0	↑	1	-	1	1	1	0	1	1	1	0	(EEh)	Reserved for future using	
		1	↑	1	-											
					-	0	0	0	0	0	0	0	0			
Reserved		0	↑	1	-	1	1	1	0	1	1	1	1	(EFh)	Reserved for future using	
		1	↑	1	-											
					-	0	0	0	0	0	0	0	0			

"-": Don't care

Note 1: E0-E7 registers are fixed for about Gamma adjusting.

Note 2: The E8h to EFh are reserved for future using.

Table 6.2.1 Panel Function Command List (5)

Instruction	Refer	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
Reserved		0	↑	1	-	1	1	1	0	0	0	0	0	(F0h)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Reserved		0	↑	1	-	1	1	1	0	0	0	0	0	(F1h)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
GAMCTRL		0	↑	1	-	1	1	1	0	0	0	1	0	(F2h)	Gamma selection
		1	↑	1	-										
					-	0	0	0	0	0	0	0	GAM_R_SEL		
Reserved		0	↑	1	-	1	1	1	0	0	0	1	1	(F3h)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Reserved		0	↑	1	-	1	1	1	0	0	1	0	0	(F4h)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Reserved		0	↑	1	-	1	1	1	0	0	1	0	1	(F5h)	Reserved for future using
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	0	0	1	1	0	(F6h)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	0	0	1	1	1	(F7h)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	0	1	0	0	0	(F8h)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	0	1	0	0	1	(F9h)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	0	1	0	1	0	(FAh)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	0	1	0	1	1	(FBh)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	0	1	1	0	0	(FCh)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	0	1	1	0	1	(FDh)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	0	1	1	1	0	(FEh)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	0	1	1	1	1	(FFh)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		

"-": Don't care

Note 1: F6h to FFh registers are reserved for about special or chip test using
Note 2: The F0h to F5h registers are reserved for future using

6.2.1 RGBCTR (B0h): RGB signal control

B0h	RGBCTR (Set RGB signal control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RGBCTR	0	↑	1	-	1	0	1	1	0	0	0	0	(B0h)
1st Parameter	1	↑	1	-	0	0	0	ICM	DP	EP	HSP	VSP	00h

NOTE: "-" Don't care

Description

-Set the operation status on the RGB interface. The setting becomes effective as soon as the command is received.

-ICM: GRAM Write/Read frequency and data input select on the RGB interface

ICM	Write/ Read frequency and input data select		
	Write cycle	Read cycle	Data input
0	PCLK	PCLK	D[17:0]
1	SCL	Internal oscillator	SDA

Symbol	Name	Clock polarity set for RGB Interface
DP	PCLK polarity set	'1' = data fetched at the falling edge '0' = data fetched at the rising edge
EP	Enable polarity set	'1' = Low enable for RGB interface '0' = High enable for RGB interface
HSP	Hsync polarity set	'1' = High level sync clock '0' = Low level sync clock
VSP	Vsync polarity set	'1' = High level sync clock '0' = Low level sync clock

Restriction

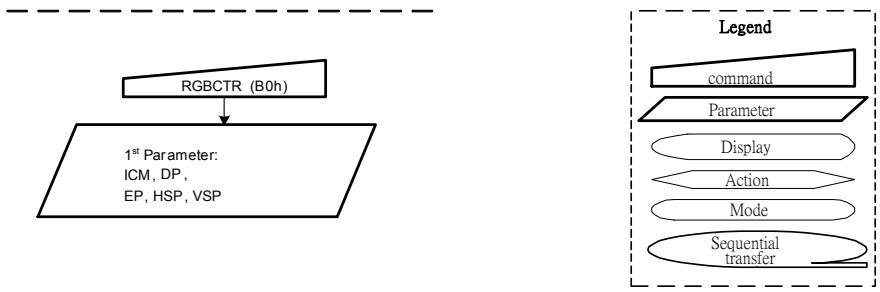
-If this register not using the register need be reserved.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	ICM	DW	DP/EP/HSP/VSP
Power On Sequence	0d	0d	0d/0d/0d/0d
S/W Reset	0d	0d	0d/0d/0d/0d
H/W Reset	0d	0d	0d/0d/0d/0d

Flow Chart	

6.2.2 FRMCTR1 (B1h): Frame Rate Control (In normal mode/ Full colors)

B1h	FRMCTR1 (In normal mode/full color)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
FRMCTR1	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)
1st Parameter	1	↑	1	-	-	-	DIVA5	DIVA4	DIVA3	DIVA2	DIVA1	DIVA0	-
2ndParameter	1	↑	1	-	-	-	VPA5	VPA4	VPA3	VPA2	VPA1	VPA0	-

NOTE: "-" Don't care

Description

Sets the division ratio for internal clocks of Normal mode and Partial mode at CPU interface mode.
DIVA[4:0]: division ratio for internal clocks when Normal mode.

VPA[5:0]: Vsync porch for internal clocks when Normal mode.

(1) When GM=00(176*220)

In Normal mode, DIVA[5:0] default value=16, line=220, VPA[5:0]=24

$$Frame\_rate = \frac{\frac{187.5KHz}{DIVA[4:0]}}{(220 + VPA[5:0])} = 60Hz$$

(2) When GM=01(176*176)

In Normal mode, DIVA[5:0] default value=20, line=176, VPA[5:0]=19

$$Frame\_rate = \frac{\frac{187.5KHz}{DIVA[4:0]}}{(176 + VPA[5:0])} = 64.11Hz$$

(3) When GM=01(176*132)

In Normal mode, DIVA[5:0] default value=27, line=132, VPA[5:0]=12

$$Frame\_rate = \frac{\frac{187.5KHz}{DIVA[4:0]}}{(132 + VPA[5:0])} = 60.1Hz$$

Restriction

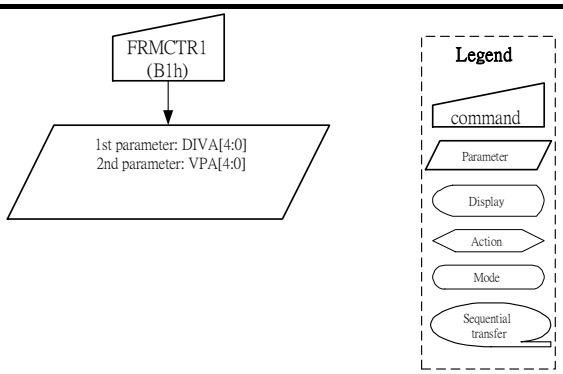
-

Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value					
GM	"00"		"01"		"11"	
	DIVA[5:0]	VPA[5:0]	DIVA[5:0]	VPA[5:0]	DIVA[5:0]	VPA[5:0]
Power On Sequence	10h	18h	14h	13h	1Bh	0Ch
S/W Reset	10h	18h	14h	13h	1Bh	0Ch
H/W Reset	10h	18h	14h	13h	1Bh	0Ch

Flow Chart	

6.2.3 FRMCTR2 (B2h): Frame Rate Control (In Idle mode/ 8-color)

B2h	FRMCTR2 (In idle mode/8-color)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
FRMCTR1	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)
1st Parameter	1	↑	1	-	-	-	DIVB5	DIVB4	DIVB3	DIVB2	DIVB1	DIVB0	-
2ndParameter	1	↑	1	-	-	-	VPB5	VPB4	VPB3	VPB2	VPB1	VPB0	-

NOTE: "-" Don't care

Description

Sets the division ratio for internal clocks of Normal mode and Partial mode at CPU interface mode.
DIVB[4:0]: division ratio for internal clocks when Partial mode.
VPB[5:0]: Vsync porch for internal clocks when Partial mode.

(1) When GM=00(176*220)

In 8-color mode, DIVA[5:0] default value=25, line=220, VPA[5:0]=14

$$Frame\_rate = \frac{\frac{187.5KHz}{DIVA[4:0]}}{(220 + VPA[5:0])} = 40.06Hz$$

(2) When GM=01(176*176)

In 8-color mode, DIVA[5:0] default value=31, line=176, VPA[5:0]=13

$$Frame\_rate = \frac{\frac{187.5KHz}{DIVA[4:0]}}{(176 + VPA[5:0])} = 40.11Hz$$

(4) When GM=01(176*132)

In 8-color mode, DIVA[5:0] default value=42, line=132, VPA[5:0]=7

$$Frame\_rate = \frac{\frac{187.5KHz}{DIVA[4:0]}}{(132 + VPA[5:0])} = 40.18Hz$$

Restriction

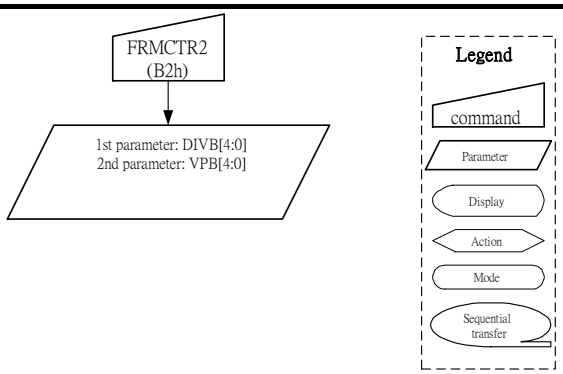
-

Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value					
GM	"00"		"01"		"11"	
	DIVA[5:0]	VPA[5:0]	DIVA[5:0]	VPA[5:0]	DIVA[5:0]	VPA[5:0]
Power On Sequence	19h	0Eh	1Fh	0Dh	2Ah	07h
S/W Reset	19h	0Eh	1Fh	0Dh	2Ah	07h
H/W Reset	19h	0Eh	1Fh	0Dh	2Ah	07h

Flow Chart	

6.2.4 FRMCTR3 (B3h): Frame Rate Control (In Partial mode/ full colors)

B3h	FRMCTR3 (In Partial mode/ full colors)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
FRMCTR3	0	↑	1	-	1	0	1	1	0	0	1	1	(B3h)
1st Parameter	1	↑	1	-	-	-	DIVC5	DIVC4	DIVC3	DIVC2	DIVC1	DIVC0	-
2ndParameter	1	↑	1	-	-	-	VPC5	VPC4	VPC3	VPC2	VPC1	VPC0	-

NOTE: "-" Don't care

Description

Sets the division ratio for internal clocks of Normal mode and Partial mode at CPU interface mode.
DIVC[4:0]: division ratio for internal clocks when Partial mode.
VPC[5:0]: Vsync porch for internal clocks when Partial mode.

(1) When GM=00(176*220)

In Partial mode, DIVA[5:0] default value=16, line=220, VPA[5:0]=24

$$Frame\_rate = \frac{\frac{187.5KHz}{DIVA[4:0]}}{(220 + VPA[5:0])} = 60Hz$$

(2) When GM=01(176*176)

In Partial mode, DIVA[5:0] default value=20, line=176, VPA[5:0]=19

$$Frame\_rate = \frac{\frac{187.5KHz}{DIVA[4:0]}}{(176 + VPA[5:0])} = 60.11Hz$$

(5) When GM=01(176*132)

In Partial mode, DIVA[5:0] default value=27, line=132, VPA[5:0]=12

$$Frame\_rate = \frac{\frac{187.5KHz}{DIVA[4:0]}}{(132 + VPA[5:0])} = 60.1Hz$$

Restriction

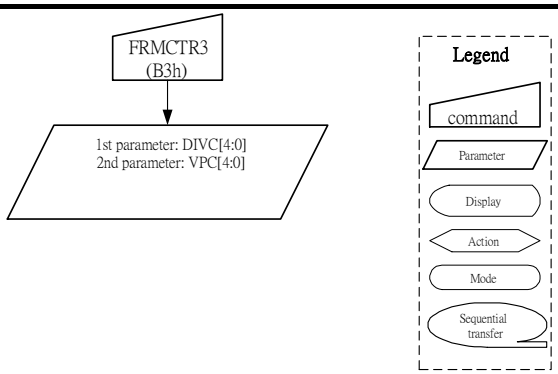
-

Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value					
GM	"00"		"01"		"11"	
	DIVA[5:0]	VPA[5:0]	DIVA[5:0]	VPA[5:0]	DIVA[5:0]	VPA[5:0]
Power On Sequence	10h	18h	14h	13h	1Bh	0Ch
S/W Reset	10h	18h	14h	13h	1Bh	0Ch
H/W Reset	10h	18h	14h	13h	1Bh	0Ch

Flow Chart	

6.2.5 INVCTR (B4h): Display Inversion Control

B4H	INVCTR (Display Inversion Control)												
Inst/Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVCTR	0	↑	1	-	1	0	1	1	0	1	0	0	(B4h)
1st Parameter	1	↑	1	-	0	0	0	0	0	NLA	NLB	NLC	02h

NOTE: "-" Don't care

Description

-Display Inversion mode control

-NLA: Inversion setting in full colors normal mode (Normal mode on)

NLA	Inversion setting in full colors normal mode
0	Line Inversion
1	Frame Inversion

-NLB: Inversion setting in Idle mode (Idle mode on)

NLB	Inversion setting in Idle mode
0	Line Inversion
1	Frame Inversion

-NLC: Inversion setting in full colors partial mode (Partial mode on / Idle mode off)

NLC	Inversion setting in full colours partial mode
0	Line Inversion
1	Frame Inversion

Restriction

-If this register not using the register need be reserved.

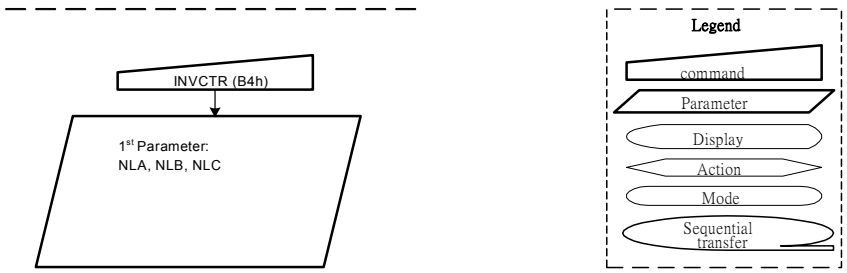
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	NLA	NLB	NLC	D7-0
Power On Sequence	0d	1d	0d	02h
S/W Reset	0d	1d	0d	02h
H/W Reset	0d	1d	0d	02h

Flow Chart



6.2.6 RGBBPCTR (B5h): RGB Interface Blanking Porch setting

B5H	RGBPSET (RGB Interface Blanking Porch setting)												
Inst/Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RGBBPCTR	0	↑	1	-	1	0	1	1	0	1	0	1	(B5h)
1st Parameter	1	↑	1	-	-	-	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	08h
2nd Parameter	1	↑	1	-	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	03h
3rd Parameter	1	↑	1	-	-	-	-	-	-	-	VBP9	VBP8	00h

NOTE: "-" Don't care

Description

Vertical and Horizontal back porch control when RGB I/F mode 2 (RCM[1:0]=11)

HBP[5:0]: Set the delay period from falling edge of HSYNC signal to first valid data.

HBP[5:0]	No. of clock cycle of DOTCLK
00d	2
01d	3
02d	4
03d	5
04d	6
05d	7
06d	8
07d	9
08d	**10**
:	:
:	(STEP 1)
:	:
62d	64
63d	65

VBP[9:0]: Set the delay period from falling edge of VSYNC signal to first valid line.

VBP[9:0]	No. of clock cycle of HSYNC
00d	(invalid)
01d	1
02d	2
03d	**3**
:	:
:	(STEP 1)
:	:
1022d	1022
1023d	1023

Restriction

-

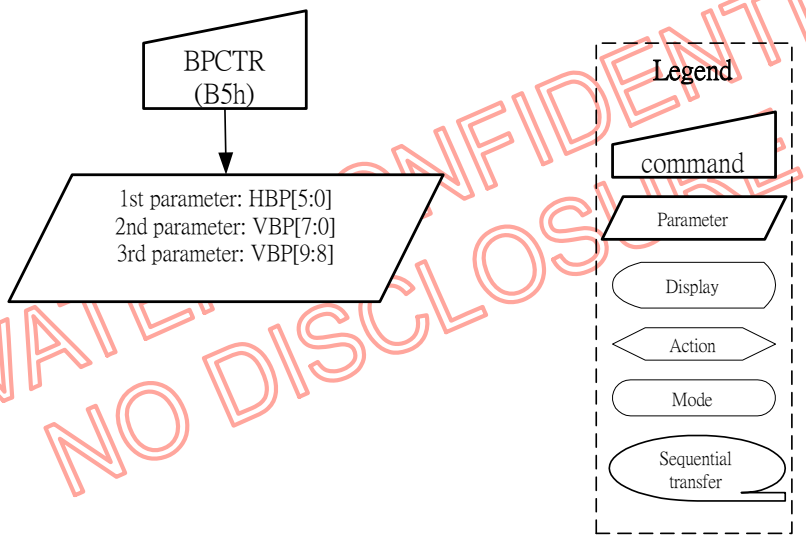
Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	HBP[5:0]	VBP[9:0]
Power On Sequence	08h	03h
S/W Reset	08h	03h
H/W Reset	08h	03h

Flow Chart



6.2.7 DISSET5 (B6h): Display Function setting

B6H	DISSET5 (Display Function setting)												
Inst/Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISSET5	0		1	-	1	0	1	1	0	1	1	0	(B6h)
1st Parameter	1	↑	1	-	0	0	NO1	NO0	SDT1	STD0	EQ1	EQ0	06h
2nd Parameter	1	↑	1	-	0	0	0	0	PTG1	PTG0	PT1	PT0	02h

NOTE: "-" Don't care

Description

-1st parameter: Set output waveform relation.

-**NO[1:0]**: Set the amount of non-overlap of the gate output

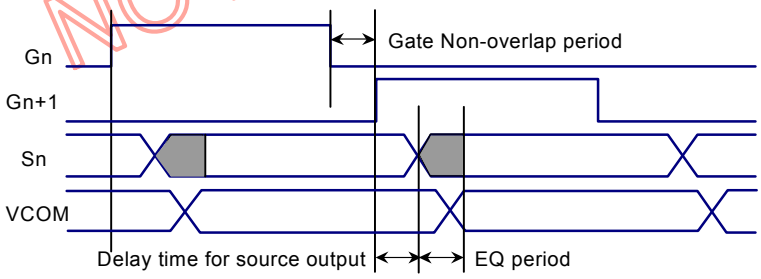
NO[1:0]		Amount of non-overlap of the gate output	
		Refer the Internal oscillator	Refer the PCLK
00	0	1 clock cycle	4 clock cycle
01	1	4 clock cycle	16 clock cycle
10	2	6 clock cycle	24 clock cycle
11	3	8 clock cycle	32 clock cycle

-**SDT[1:0]**: Set delay amount from gate signal falling edge of the source output.

SDT[1:0]		Amount of non-overlap of the source output	
		Refer the Internal oscillator	Refer the PCLK
00	0	1 clock cycle	4 clock cycle
01	1	2 clock cycle	8 clock cycle
10	2	3 clock cycle	12 clock cycle
11	3	4 clock cycle	16 clock cycle

-**EQ[1:0]**: Set the Equalizing period

EQ[1:0]		EQ period	
		Refer the Internal oscillator	Refer the PCLK
00	0	No EQ	No EQ
01	1	2 clock cycle	4 clock cycle
10	2	4 clock cycle	16 clock cycle
11	3	6 clock cycle	24 clock cycle



-2nd parameter: Set the output waveform in non-display area.

-**PTG[1:0]**: Determine gate output in a non-display area in the partial mode

PTG[1:0]		Gate output in a non-display area
00	0	Normal scan
01	1	Fix on VGL
10	2	Fix on VGL
11	3	Fix on VGL

-**PT[1:0]**: Determine Source /VCOM output in a non-display area in the partial mode

PT[1:0]		Source output on non-display area		VCOM output on non-display area	
		Positive	Negative	Positive	Negative
00	0	V63	V0	VCOML	VCOMH
01	1	V0	V63	VCOML	VCOMH
10	2	AGND	AGND	AGND	AGND
11	3	Hi-z	Hi-z	AGND	AGND

Restriction

-If this register not using the register need be reserved.

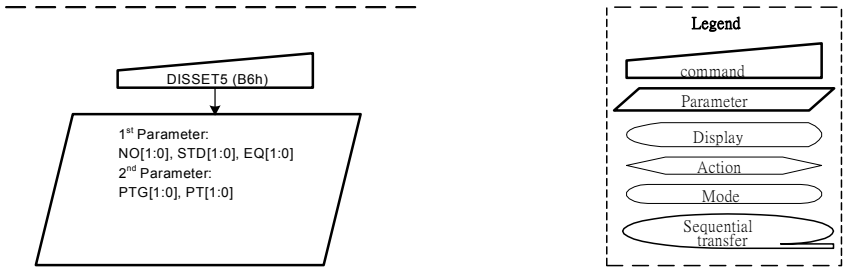
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value				
	NO[1:0]	STD[1:0]	EQ[1:0]	PTG[1:0]	PT[1:0]
Power On Sequence	0d	1d	2d	0d	2d
S/W Reset	0d	1d	2d	0d	2d
H/W Reset	0d	1d	2d	0d	2d

Flow Chart



6.2.8 DISSET6 (B7h): Source Driver Output Direction Control

B7H	DISSET6 (Source Driver Output Direction Control)												
Inst/Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISSET6	0	↑	1	-	1	0	1	1	0	1	1	1	(B7h)
1st Parameter	1	↑	1	-	0	0	0	0	0	0	0	CRL	00h

NOTE: "-" Don't care

Description

-CRL: Source output direction select register in RGB I/F (GM="00","01","11")

CRL	Module source output direction
0	S1~S528
1	S528~S1

-Please refer RGB I/F for detail using.

Restriction

-If this register not using the register need be reserved.

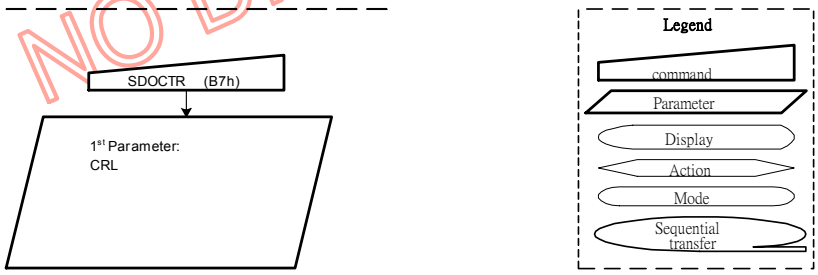
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	CRL
Power On Sequence	0h
S/W Reset	0h
H/W Reset	0h

Flow Chart



6.2.9 DISSET7 (B8h): Gate Driver Output Direction Control

B4H	INVCTR (Gate Driver Output Direction Control)												
Inst/Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISSET7	0	↑	1	-	1	0	1	1	0	1	1	1	(B8h)
1st Parameter	1	↑	1	-	0	0	0	0	0	0	0	CTB	00h

NOTE: "-" Don't care

Description

-CTB: Gate output direction select register on RGB I/F

CTB	Module Gate output direction		
	GM=00	GM=01	GM=11
0	**G1** -> G220	**G1** -> G176	**G1** -> G132
1	G220 -> **G1**	G176 -> **G1**	G132 -> **G1**

-Please refer RGB I/F for detail using.

Restriction

-If this register not using the register need be reserved.

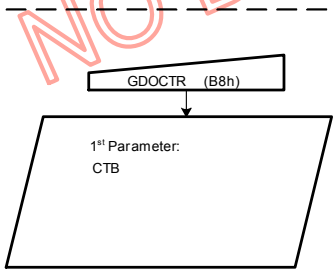
Register Availability

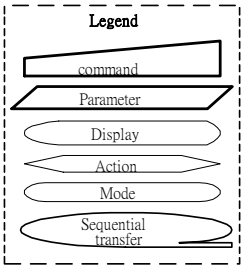
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	CTB
Power On Sequence	0h
S/W Reset	0h
H/W Reset	0h

Flow Chart





6.2.10 PWCTR1 (C0h): Power Control 1

C0H	PWCTR1 (Power Control 1)												
Inst/Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR1	0	↑	1	-	1	1	0	0	0	0	0	0	(C0h)
1st Parameter	1	↑	1	-	0	0	0	VRH4	VRH3	VRH2	VRH1	VRH0	05h/05h
2nd Parameter	1	↑	1	-	0	0	0	0	0	VC2	VC1	VC0	05h/05h

NOTE: "-" Don't care

Description

- -Set the GVDD and voltage

VRH[4:0]		GVDD
00000	0	5.00
00001	1	4.75
00010	2	4.70
00011	3	4.65
00100	4	4.60
00101	5	**4.55**
00110	6	4.50
00111	7	4.45
01000	8	4.40
01001	9	4.35
01010	10	4.30
01011	11	4.25
01100	12	4.20
01101	13	4.15
01110	14	4.10
01111	15	4.05
10000	16	4.00
10001	17	3.95
10010	18	3.90
10011	19	3.85
10100	20	3.80
10101	21	3.75
10110	22	3.70
10111	23	3.65
11000	24	3.60
11001	25	3.55
11010	26	3.50
11011	27	3.45
11100	28	3.40
11101	29	3.35
11110	30	3.25
11111	31	3.00

VC[2:0]		VCI1
000	0	2.75
001	1	2.70
010	2	2.65
011	3	2.60
100	4	2.55
101	5	**2.5**
110	6	2.45
111	7	2.4

Restriction

-If this register not using the register need be reserved.
-The deviation value of GVDD between with Measurement and Specification: **Max <=50mV**
-The deviation value of VCI1 between with Measurement and Specification: **Max <= 2%**

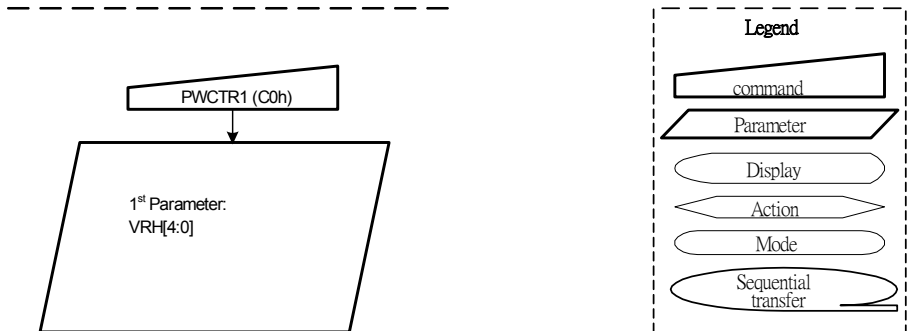
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	LCM = "01"		LCM = "11"	
	TM LC Type		ECB LC type	
	VRH[4:0]	VC[2:0]	VRH[4:0]	VC[2:0]
Power On Sequence	05h	05h	05h	05h
S/W Reset	05h	05h	05h	05h
H/W Reset	05h	05h	05h	05h

Flow Chart



6.2.11 PWCTR2 (C1h): Power Control 2

C1H	PWCTR2 (Power Control 2)												
Inst/Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR2	0	↑	1	-	1	1	0	0	0	0	0	1	(C1h)
1st Parameter	1	↑	1		0	0	0	0	0	BT2	BT1	BT0	07h

NOTE: "-" Don't care

Description

- Set the AVDD, VCL, VGH and VGL supply power level

BT[2:0]		AVDD	VCL	VGH	VGL
000	0	4.75	-2.45	4xVCI1	-3xVCI1
001	1	4.75	-2.45	4xVCI1	-4xVCI1
010	2	4.75	-2.45	5xVCI1	-3xVCI1
011	3	4.75	-2.45	5xVCI1	-4xVCI1
100	4	4.75	-2.45	5xVCI1	-5xVCI1
101	5	4.75	-2.45	6xVCI1	-3xVCI1
110	6	4.75	-2.45	6xVCI1	-4xVCI1
111	7	**4.75**	**-2.45**	6xVCI1	-5xVCI1

Note: When VCI1=2.5V

Restriction

-If this register not using the register need be reserved.
-The deviation value of VGH/ VGL between with Measurement and Specification:
-VGH-VGL <= 25V

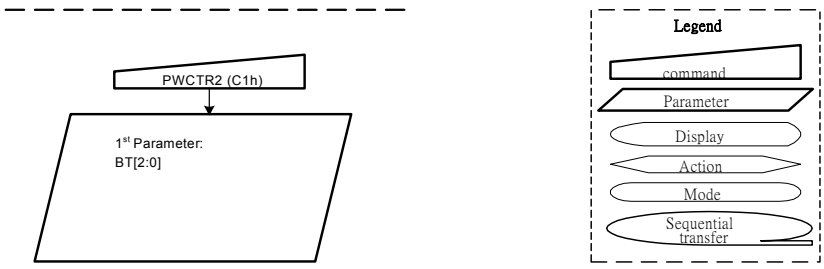
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	BT[2:0]
Power On Sequence	07h
S/W Reset	07h
H/W Reset	07h

Flow Chart



6.2.12 PWCTR3 (C2h): Power Control 3 (in Normal mode/ Full colors)

C2H	PWCTR3 (Power Control 3)												
Inst/Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR3	0	↑	1	-	1	1	0	0	0	0	1	0	(C2h)
1st Parameter	1	↑	1		0	0	0	0	0	APA2	APA1	APA0	04h
2nd Parameter	1	↑	1		0	0	0	0	0	DCA2	DCA1	DCA0	06h

NOTE: "-" Don't care

Description

-Set the amount of current in Operational amplifier in normal mode/full colors.
-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.

APA[2:0]		Amount of Current in Operational Amplifier
000	0	Operation of the operational amplifier stops
001	1	Small
010	2	Medium Low
011	3	Medium
100	**4**	**Medium High**
101	5	Large
110	6	Reserved
111	7	Reserved

-Set the Booster circuit Step-up cycle in Normal mode/ full colors.

DCA[2:0]		Step-up cycle in Booster circuit 1	Step-up cycle in Booster circuit 2,3
000	0	BCLK / 1	BCLK / 4
001	1	BCLK / 1	BCLK / 8
010	2	BCLK / 1	BCLK / 16
011	3	BCLK / 2	BCLK / 16
100	4	BCLK / 4	BCLK / 16
101	5	BCLK / 4	BCLK / 32
110	**6**	**BCLK / 4**	**BCLK / 64**
111	7	BCLK / 8	BCLK / 64

Note: BCLK is Clock frequency for Booster circuit

Restriction

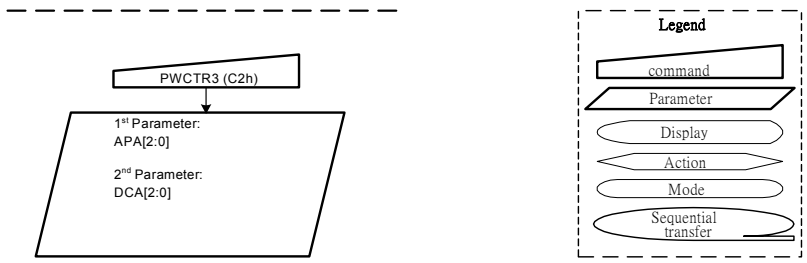
-If some parameter of the register not use the register need to be reserved.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	APA[2:0]	DCA[2:0]
Power On Sequence	02h	04h
S/W Reset	02h	04h
H/W Reset	02h	04h

Flow Chart	

6.2.13 PWCTR4 (C3h): Power Control 4 (in Idle mode/ 8-colors)

C3H	PWCTR4 (Power Control 4)												
Inst/Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR4	0	↑	1	-	1	1	0	0	0	0	1	1	(C3h)
1st Parameter	1	↑	1		0	0	0	0	0	APB2	APB1	APB0	04h
2nd Parameter	1	↑	1		0	0	0	0	0	DCB2	DCB1	DCB0	07h

NOTE: "-" Don't care

Description

-Set the amount of current in Operational amplifier in Idle mode/ 8-colors.
-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.

APB[2:0]		Amount of Current in Operational Amplifier
000	0	Operation of the operational amplifier stops
001	1	Small
010	2	Medium Low
011	3	Medium
100	**4**	**Medium High**
101	5	Large
110	6	Reserved
111	7	Reserved

-Set the Booster circuit Step-up cycle in Idle mode/ 8-colors.

DCB[2:0]		Step-up cycle in Booster circuit 1	Step-up cycle in Booster circuit 2,3
000	0	BCLK / 1	BCLK / 4
001	1	BCLK / 1	BCLK / 8
010	2	BCLK / 1	BCLK / 16
011	3	BCLK / 2	BCLK / 16
100	4	BCLK / 4	BCLK / 16
101	5	BCLK / 4	BCLK / 32
110	6	BCLK / 4	BCLK / 64
111	**7**	**BCLK / 8**	**BCLK / 64**

Note: BCLK is Clock frequency for Booster circuit

Restriction

-If some parameter of the register not use, the register need to be reserved.

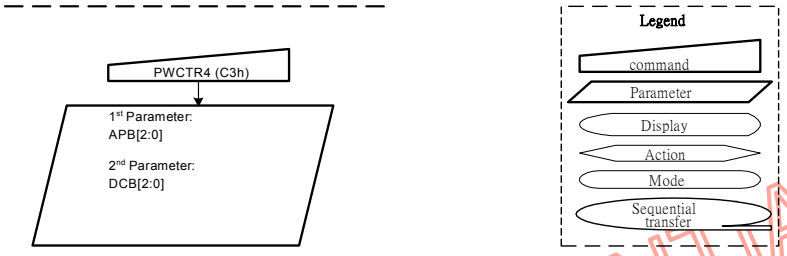
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	AP[2:0]	DC[2:0]
Power On Sequence	02h	07h
S/W Reset	02h	07h
H/W Reset	02h	07h

Flow Chart



6.2.14 PWCTR5 (C4h): Power Control 5 (in Partial mode/ full-colors)

C4H	PWCTR5 (Power Control 5)												
Inst/Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR5	0	↑	1	-	1	1	0	0	0	1	0	0	(C4h)
1st Parameter	1	↑	1		0	0	0	0	0	APC2	APC1	APC0	03h
2nd Parameter	1	↑	1		0	0	0	0	0	DCC2	DCC1	DCC0	07h

NOTE: "-" Don't care

Description

-Set the amount of current in Operational amplifier in Partial mode/ full-colors.
-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.

APC[2:0]		Amount of Current in Operational Amplifier
000	0	Operation of the operational amplifier stops
001	1	Small
010	2	Medium Low
011	**3**	**Medium**
100	4	Medium High
101	5	Large
110	6	Reserved
111	7	Reserved

-Set the Booster circuit Step-up cycle in Partial mode/ full-colors.

DCC[2:0]		Step-up cycle in Booster circuit 1	Step-up cycle in Booster circuit 2,3
000	0	BCLK / 1	BCLK / 4
001	1	BCLK / 1	BCLK / 8
010	2	BCLK / 1	BCLK / 16
011	3	BCLK / 2	BCLK / 16
100	4	BCLK / 4	BCLK / 16
101	5	BCLK / 4	BCLK / 32
110	6	BCLK / 4	BCLK / 64
111	**7**	**BCLK / 8**	**BCLK / 64**

Note: BCLK is Clock frequency for Booster circuit

Restriction

-If some parameter of the register not use the register need to be reserved.

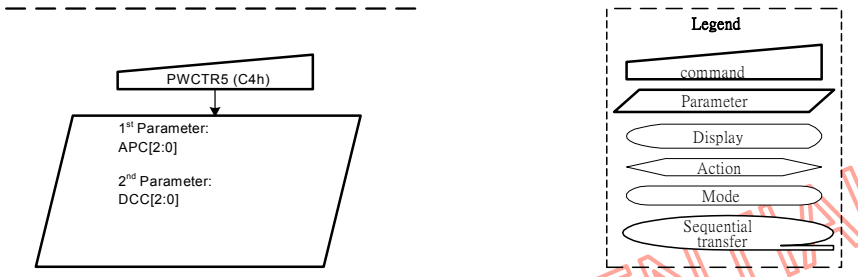
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	AP[2:0]	DC[2:0]
Power On Sequence	02h	04h
S/W Reset	02h	04h
H/W Reset	02h	04h

Flow Chart



6.2.15 VMCTR1 (C5h): VCOM Control 1

C5H	VMCTR1 (VCOM Control 1)												
Inst/Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VMCTR1	0	↑	1	-	1	1	0	0	0	1	0	1	(C5h)
1st Parameter	1	↑	1		-	VMH6	VMH5	VMH4	VMH3	VMH2	VMH1	VMH0	1Ah/3Ah
2nd Parameter	1	↑	1		0	VML6	VML5	VML4	VML3	VML2	VML1	VML0	18h/38h

NOTE: "-" Don't care

Description

-Set VCOMH Voltage

VMH[6:0]		VCOMH	VMH[6:0]		VCOMH	VMH[6:0]		VCOMH	VMH[6:0]		VCOMH
0000000	0	2.500	0011011	27	3.175	0110110	54	3.850	1010001	81	4.525
0000001	1	2.525	0011100	28	3.200	0110111	55	3.875	1010010	82	4.550
0000010	2	2.550	0011101	29	3.225	0111000	56	3.900	1010011	83	4.575
0000011	3	2.575	0011110	30	3.250	0111001	57	3.925	1010100	84	4.600
0000100	4	2.600	0011111	31	3.275	**0111010**	**58**	3.950(ECB)	1010101	85	4.625
0000101	5	2.625	0100000	32	3.300	0111011	59	3.975	1010110	86	4.650
0000110	6	2.650	0100001	33	3.325	0111100	60	4.000	1010111	87	4.675
0000111	7	2.675	0100010	34	3.350	0111101	61	4.025	1011000	88	4.700
0001000	8	2.700	0100011	35	3.375	0111110	62	4.050	1011001	89	4.725
0001001	9	2.725	0100100	36	3.400	0111111	63	4.075	1011010	90	4.750
0001010	10	2.750	0100101	37	3.425	1000000	64	4.100	1011011	91	4.775
0001011	11	2.775	0100110	38	3.450	1000001	65	4.125	1011100	92	4.800
0001100	12	2.800	0100111	39	3.475	1000010	66	4.150	1011101	93	4.825
0001101	13	2.825	0101000	40	3.500	1000011	67	4.175	1011110	94	4.850
0001110	14	2.850	0101001	41	3.525	1000100	68	4.200	1011111	95	4.875
0001111	15	2.875	0101010	42	3.550	1000101	69	4.225	1100000	96	4.900
0010000	16	2.900	0101011	43	3.575	1000110	70	4.250	1100001	97	4.925
0010001	17	2.925	0101100	44	3.600	1000111	71	4.275	1100010	98	4.950
0010010	18	2.950	0101101	45	3.625	1001000	72	4.300	1100011	99	4.975
0010011	19	2.975	0101110	46	3.650	1001001	73	4.325	1100100	100	5.000
0010100	20	3.000	0101111	47	3.675	1001010	74	4.350	1100101	101	Not
0010101	21	3.025	0110000	48	3.700	1001011	75	4.375		|	Permitted
0010110	22	3.050	0110001	49	3.725	1001100	76	4.400	1111111	127	
0010111	23	3.075	0110010	50	3.750	1001101	77	4.425			
0011000	24	3.100	0110011	51	3.775	1001110	78	4.450			
0011001	25	3.125	0110100	52	3.800	1001111	79	4.475			
0011010	**26**	3.150(TM)	0110101	53	3.825	1010000	80	4.500			

*When using VCOMH lower than VDD,EQ function must turn off.

-Set VCOML Voltage

VML[6:0]		VCOML	VML[6:0]		VCOML	VML[6:0]		VCOML	VML[6:0]		VCOML
0000000	0	-2.500	0011011	27	-1.825	0110110	54	-1.150	1010001	81	-0.475
0000001	1	-2.475	0011100	28	-1.800	0110111	55	-1.125	1010010	82	-0.450
0000010	2	-2.450	0011101	29	-1.775	**0111000**	**56**	-1.100(ECB)	1010011	83	-0.425
0000011	3	-2.425	0011110	30	-1.750	0111001	57	-1.075	1010100	84	-0.400
0000100	4	-2.400	0011111	31	-1.725	0111010	58	-1.050	1010101	85	-0.375
0000101	5	-2.375	0100000	32	-1.700	0111011	59	-1.025	1010110	86	-0.350
0000110	6	-2.350	0100001	33	-1.675	0111100	60	-1.000	1010111	87	-0.325
0000111	7	-2.325	0100010	34	-1.650	0111101	61	-0.975	1011000	88	-0.300
0001000	8	-2.300	0100011	35	-1.625	0111110	62	-0.950	1011001	89	-0.275
0001001	9	-2.275	0100100	36	-1.600	0111111	63	-0.925	1011010	90	-0.250
0001010	10	-2.250	0100101	37	-1.575	1000000	64	-0.900	1011011	91	-0.225

0001011	11	-2.225	0100110	38	-1.550	1000001	65	-0.875	1011100	92	-0.200
0001100	12	-2.200	0100111	39	-1.525	1000010	66	-0.850	1011101	93	-0.175
0001101	13	-2.175	0101000	40	-1.500	1000011	67	-0.825	1011110	94	-0.150
0001110	14	-2.150	0101001	41	-1.475	1000100	68	-0.800	1011111	95	-0.125
0001111	15	-2.125	0101010	42	-1.450	1000101	69	-0.775	1100000	96	-0.100
0010000	16	-2.100	0101011	43	-1.425	1000110	70	-0.750	1100001	97	-0.075
0010001	17	-2.075	0101100	44	-1.400	1000111	71	-0.725	1100010	98	-0.050
0010010	18	-2.050	0101101	45	-1.375	1001000	72	-0.700	1100011	99	-0.025
0010011	19	-2.025	0101110	46	-1.350	1001001	73	-0.675	1100100	100	0.000
0010100	20	-2.000	0101111	47	-1.325	1001010	74	-0.650	1100101	101	Not
0010101	21	-1.975	0110000	48	-1.300	1001011	75	-0.625		|	Permitted
0010110	22	-1.950	0110001	49	-1.275	1001100	76	-0.600	1111111	127	
0010111	23	-1.925	0110010	50	-1.250	1001101	77	-0.575			
0011000	**24**	-1.900(TM)	0110011	51	-1.225	1001110	78	-0.550			
0011001	25	-1.875	0110100	52	-1.200	1001111	79	-0.525			
0011010	26	-1.850	0110101	53	-1.175	1010000	80	-0.500			

Restriction

-If this register not using the register need be reserved.
-The deviation value of VCOMH/VCOML between with Measurement and Specification: **Max<=25mV**
-The deviation value of VCOMAC between with Measurement and Specification: **Max <=50mV**

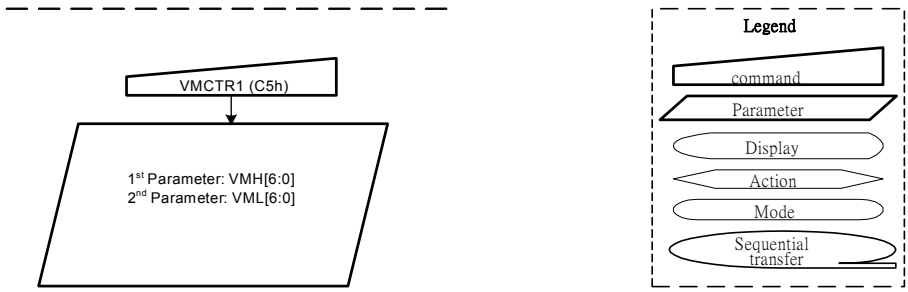
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	nVM	LCM = "01" TM LC Type	LCM = "11" ECB LC type
		VMH[6:0] / VML[6:0]	VMH[6:0] / VML[6:0]
Power On Sequence	0d	1Ah/18h	3Ah/38h
S/W Reset	0d	1Ah/18h	3Ah/38h
H/W Reset	0d	1Ah/18h	3Ah/38h

Flow Chart



6.2.16 VMOFCTR (C7h): VCOM Offset Control

C7H	VMOFCTR (VCOM Offset Control)												
Inst/Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VMCTR2	0	↑	1	-	1	1	0	0	0	1	1	1	(C7h)
1st Parameter	1	↑	1		nVM*	VMF6	VMF5	VMF4	VMF3	VMF2	VMF1	VMF0	MTP

NOTE: "-" Don't care

Description

-Set VCOMH Voltage

VMF[6:0]	VCOMH Output Level	VCOML Output Level
0	"VMH" – 64d	"VML" – 64d
1	"VMH" – 63d	"VML" –63d
2	"VMH" – 62d	"VML" –62d
:	:	:
62	"VMH" –2d	"VML" –2d
63	"VMH" –1d	"VML" –1d
64	**"VMH"**	**"VML"**
65	"VMH" + 1d	"VML"+ 1d
66	"VMH" + 2d	"VML"+ 2d
:	:	:
126	"VMH"+ 62d	"VML" + 62d
127	"VMH"+ 63d	"VML" + 63d

-IF "VMH" + xd or "VML" + xd is less than 0d, it becomes 0d.
-IF "VMH" + xd or "VML" + xd is large than 100d, it becomes 100d.
-VMF[5:0] are stored in NV memory to contrast.
-
-Select the VMF[6:0] value

nVM	VMF[6:0] value
0	**VCOM offset value from NV memory**
1	VCOM offset value in the VMF[6:0] registers

-When the VCOM circuit use VCOMH (C5h) + VCOML (C5h) + VCOM-offset (C7h) structure, the nVM need to be used in this case.

Restriction

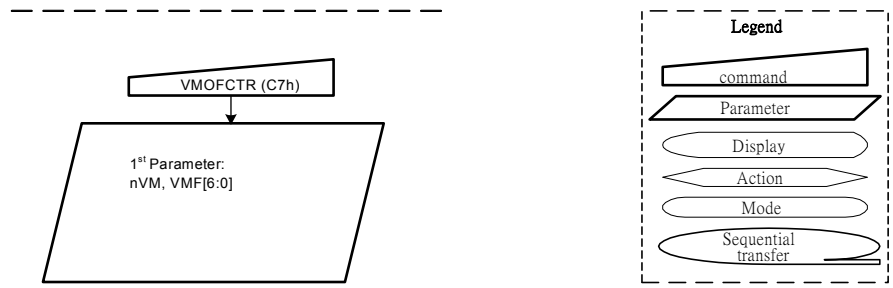
-If this register not use the register need be reserved.
-To control the VCOM output voltage with VMF[5:0] command, nVM parameter should be set '1'.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value VMF[6:0]
Power On Sequence	MTP
S/W Reset	No change
H/W Reset	MTP

Flow Chart	

6.2.17 RDVMOF (C8h): Read the VCOM Offset Value NV memory

C8H	RDVMOF (Read the VCOM Offset Value NV memory)												
Inst/ Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDVMOF	0	↑	1	-	1	1	0	0	1	0	0	0	(C8h)
1st Parameter	0	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-		RVMF6	RVMF5	RVMF4	RVMF3	RVMF2	RVMF1	RVMF0	--

NOTE: "-" Don't care

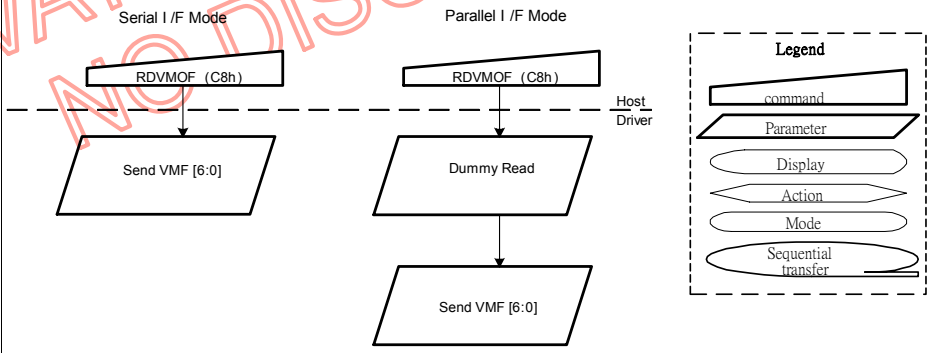
Description	-Read the VCOM offset value from NV memory -The 1st parameter is dummy data. -The 2nd parameter is VMF[6:0] value from NV memory or register value.
Restriction	-If this register not use the register need be reserved.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value VMF[5:0]
Power On Sequence	MTP
S/W Reset	MTP
H/W Reset	MTP

Flow Chart



6.2.18 WRID2 (D1h): Write ID2 Value

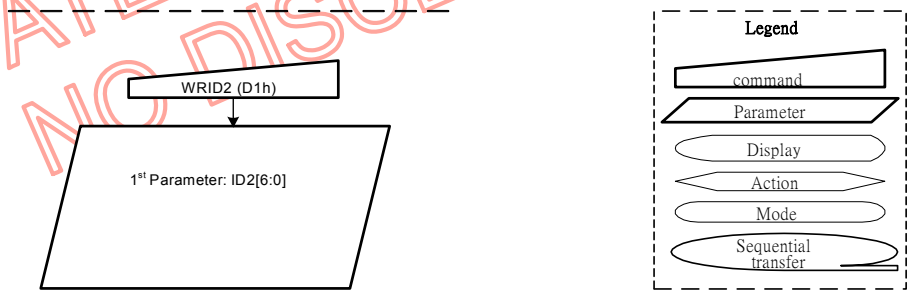
D1H	WRID2 (Write ID2 Value)												
Inst/ Para	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
WRID2	0	↑	1	-	1	1	0	1	0	0	0	1	(D1h)
1st Parameter	1	↑	1	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-

NOTE: "-" Don't care

Description	-Write 7-bits data of LCD module version to save it to NV memory. -The 1st parameter ID2[6:0] is LCD Module version ID.
Restriction	
Register Availability	
Default	
Flow Chart	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	MTP
S/W Reset	MTP
H/W Reset	MTP



6.2.19 WRID3 (D2h): Write ID3 Value

D2H	WRID3 (Write ID3 Value)												
Inst/ Para	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
WRID3	0	↑	1	-	1	1	0	1	0	0	1	0	(D2h)
1st Parameter	1	↑	1	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-

NOTE: "-" Don't care

Description

-Write 8-bits data of project code module to save it to NV memory.
-The 1st parameter ID3[7:0] is product project ID.
- The default value needs to be defined later.

Restriction

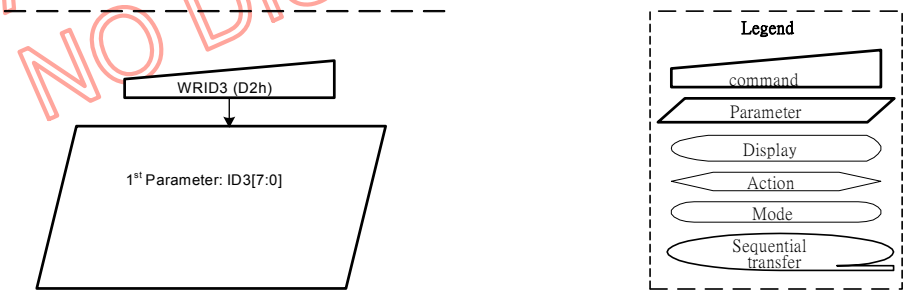
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	MTP
S/W Reset	MTP
H/W Reset	MTP

Flow Chart



6.2.20 RDID4 (D3h): Read the ID4 value

D3H	RDID4 (Read the ID4 value)												
Inst/ Para	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID4	0	↑	1	-	1	1	0	1	0	0	1	1	(D3h)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd Parameter	1	1	↑	-	ID417	ID416	ID415	ID414	ID413	ID412	ID411	ID410	01h
3rd Parameter	1	1	↑	-	ID427	ID426	ID425	ID424	ID423	ID422	ID421	ID420	16h
4th Parameter	1	1	↑	-	-	-	-	-	ID433	ID432	ID431	ID430	-

NOTE: "-" Don't care

Description

-Read the Driver IC information from mask value.
-The 1st parameter is dummy data.
-The 2nd parameter ID41[7:0] is Driver IC ID code.
-The value be defined later.
-Currently, "01h", "02h" , "03h" , "05h" can't be used.
-The 3rd parameter ID42[7:0] is Driver IC Part number ID. (The code be define by Driver IC Vender)
-The 4th parameter ID43[3:0] is Driver IC version ID.
-When the Driver maker modifies any function it should be modify the parameters at this ID code before sample out also.
-If Driver Maker don't need 2 parameter If can't reduce to one parameter.
-If the parameters are not enough Driver makers can add or reduce yourself.

Restriction

-

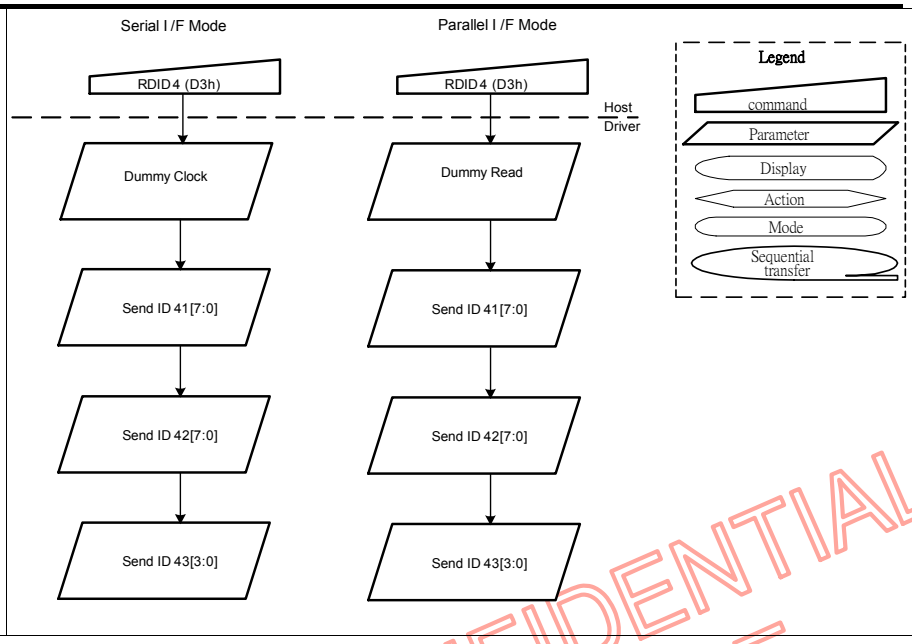
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value-		
	ID41[7:0]	ID42[7:0]	ID43[3:0]
Power On Sequence	01h	16h	02h
S/W Reset	01h	16h	02h
H/W Reset	01h	16h	02h

Flow Chart



6.2.21 NVFCTR1 (D9h): NV Memory Function Controller 1

D9H	NVFCTR1 (NV Memory Function Controller 1)												
Inst/ Para	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NVFCTR1	0	↑	1	-	1	1	0	1	1	0	0	1	(D9h)
1st Parameter	1	↑	1	-								EP_PWR	-

NOTE: "-" Don't care

Description	EP_PWR: MTP programming power control. ("0": Internal power, "1": External power form VGH) Note: The register is not used in this case.
Restriction	-

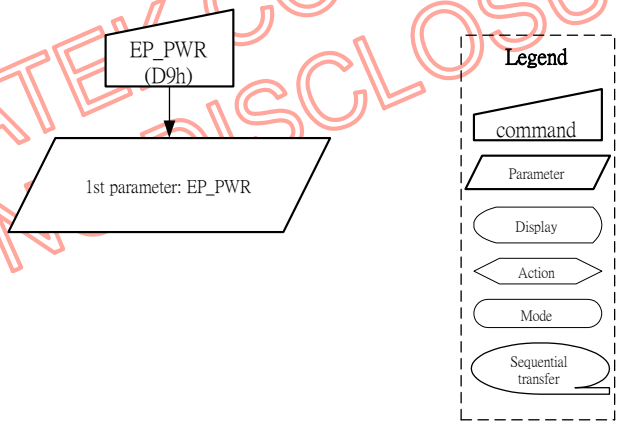
Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00
S/W Reset	00
H/W Reset	00

Flow Chart



6.2.22 EPWRITE (DEh): MTP write command

DEH	NVFCTR2 (NV Memory Function Controller 2)												
Inst/ Para	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
EPWRITE	0	↑	1	-	1	1	0	1	1	1	1	0	(DEh)

NOTE: "-" Don't care

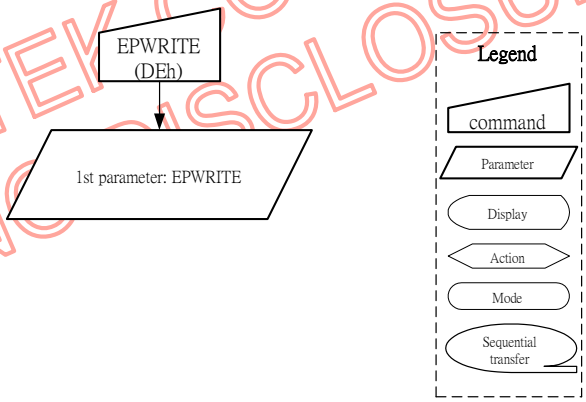
Description	MTP write command. Please see ***6.2.25 MTP Access sequence for program (Data write)*** for more detail.
Restriction	-
Register Available	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.23 EPCLR (DFh): MTP read command

DFH	NVFCTR3 (NV Memory Function Controller 3)												
Inst/ Para	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
EPCLR	0	↑	1	-	1	1	0	1	1	1	1	1	(DFh)

NOTE: "-" Don't care

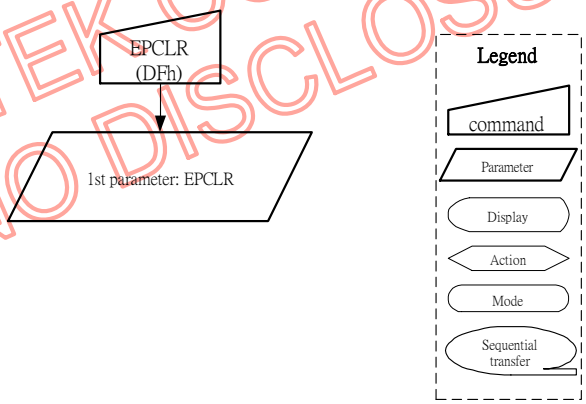
Description	MTP write command. Please see ***6.2.26 MTP Access sequence for program (Data clear)*** for more detail.
Restriction	-
Register Available	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

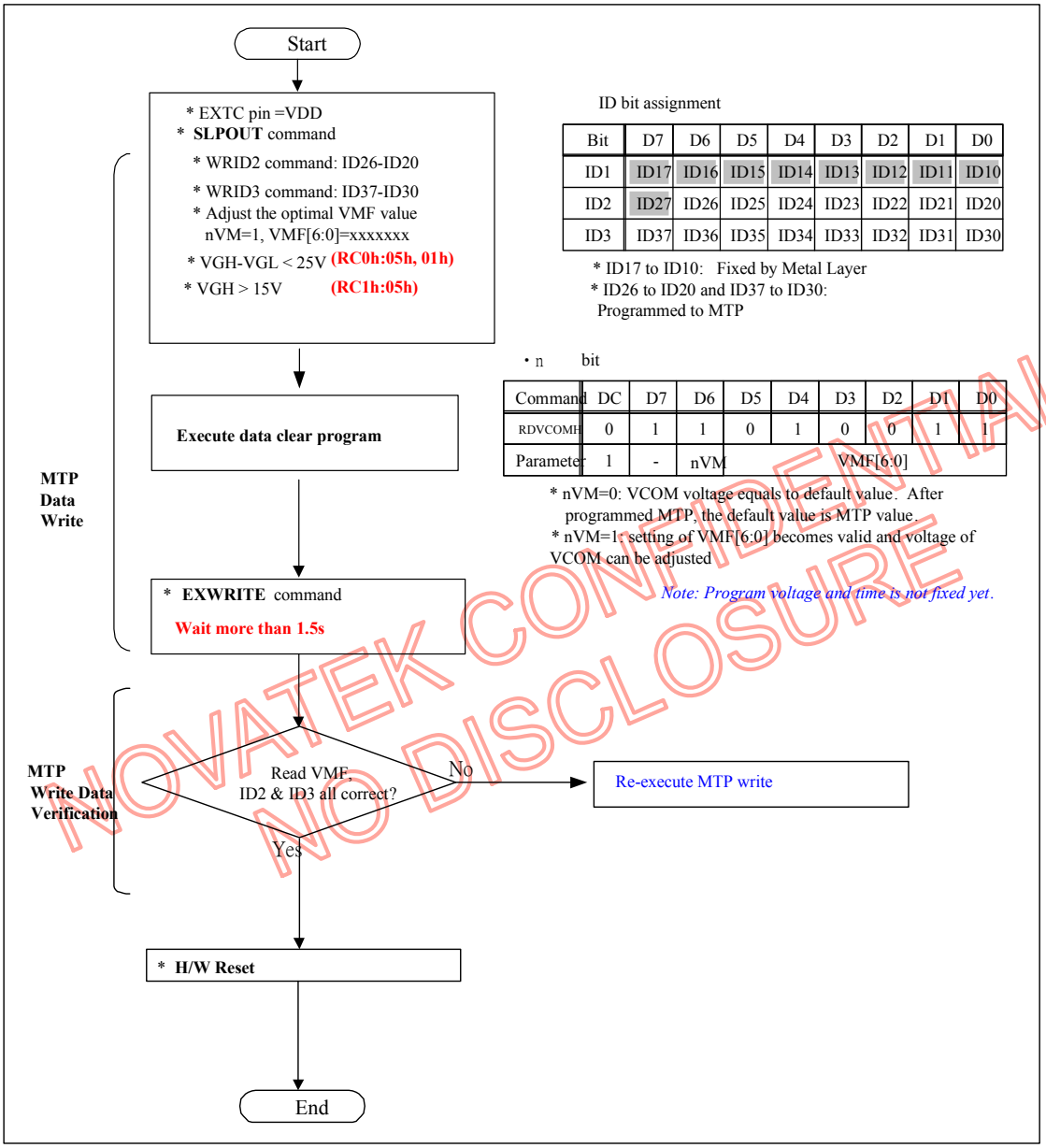
Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.24 MTP Access Sequence for Program (Data write)



ID bit assignment

Bit	D7	D6	D5	D4	D3	D2	D1	D0
ID1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10
ID2	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20
ID3	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30

* ID17 to ID10: Fixed by Metal Layer
* ID26 to ID20 and ID37 to ID30: Programmed to MTP

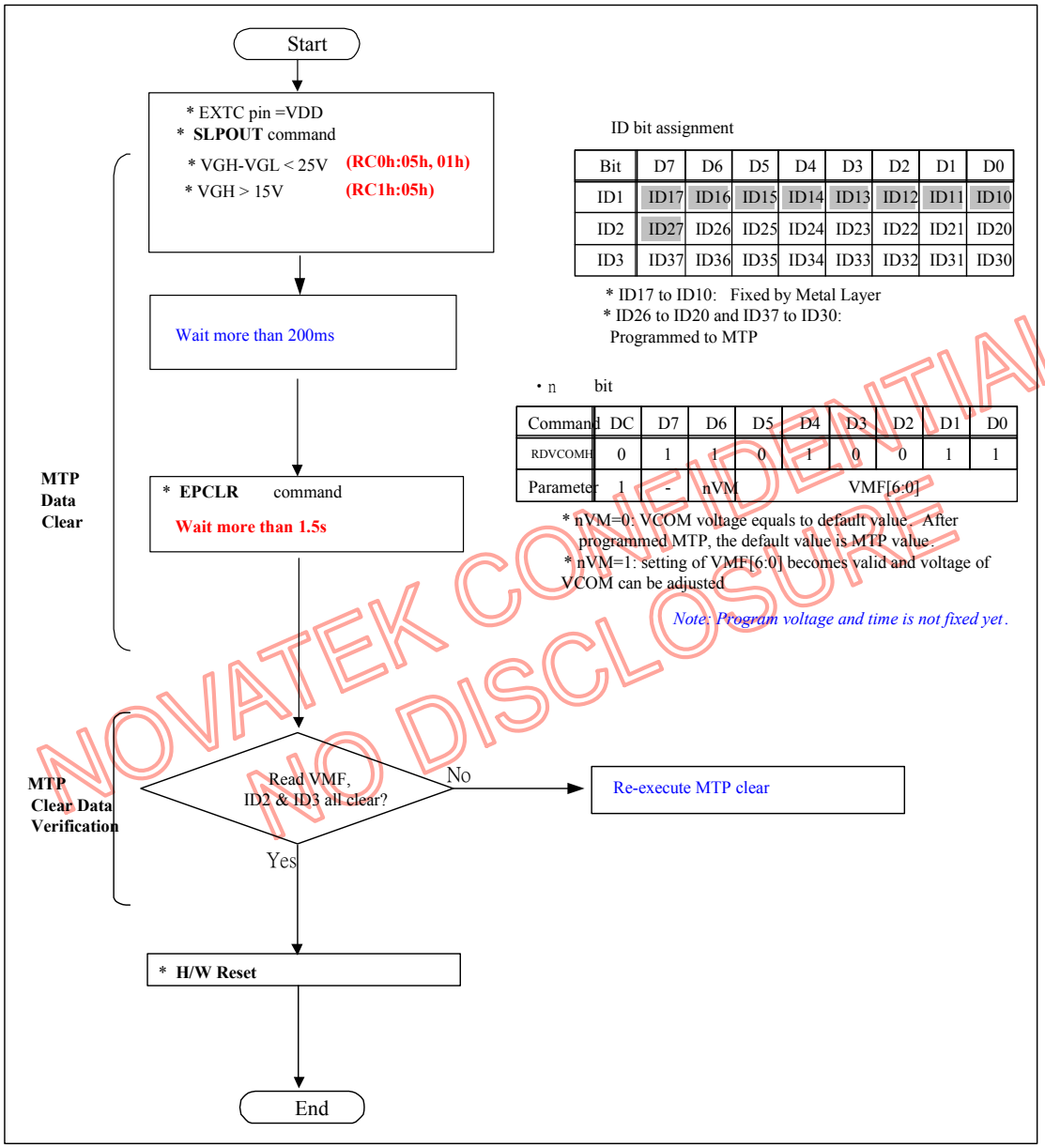
• n bit

Command	DC	D7	D6	D5	D4	D3	D2	D1	D0
RDVCOMH	0	1	1	0	1	0	0	1	1
Parameter	1	-	nVM	VMF[6:0]					

* nVM=0: VCOM voltage equals to default value. After programmed MTP, the default value is MTP value.
* nVM=1: setting of VMF[6:0] becomes valid and voltage of VCOM can be adjusted

Note: Program voltage and time is not fixed yet.

6.2.25 MTP Access Sequence for Program (Data clear)



ID bit assignment

Bit	D7	D6	D5	D4	D3	D2	D1	D0
ID1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10
ID2	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20
ID3	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30

* ID17 to ID10: Fixed by Metal Layer
* ID26 to ID20 and ID37 to ID30: Programmed to MTP

• n bit

Command	DC	D7	D6	D5	D4	D3	D2	D1	D0
RDVCOMH	0	1	1	0	1	0	0	1	1
Parameter	1	-	nVM			VMF[6:0]			

* nVM=0: VCOM voltage equals to default value. After programmed MTP, the default value is MTP value.
* nVM=1: setting of VMF[6:0] becomes valid and voltage of VCOM can be adjusted.

Note: Program voltage and time is not fixed yet.

6.2.26 GMCTRP1(E0h): Gamma (‘+’polarity) Correction Characteristics Setting

E0H	GMCTRP1(Gamma (‘+’polarity) Correction Characteristics Setting)												
Inst/ Para	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GMCTRP1	0	↑	1	-	1	1	1	1	0	0	0	0	(E0h)
1st Parameter	1	↑	1	-	-	PKP12	PKP11	PKP10	-	PKP02	PKP01	PKP00	
2nd Parameter	1	↑	1	-	-	PKP32	PKP31	PKP30	-	PKP22	PKP21	PKP20	-
3rd Parameter	1	↑	1	-	-	PKP52	PKP51	PKP50	-	PKP42	PKP41	PKP40	-
4th Parameter	1	↑	1	-	-	-	-	PRP04	PRP03	PRP02	PRP01	PRP00	-
5th Parameter	1	↑	1	-	PRP23	PRP22	PRP21	PRP20	PRP13	PRP12	PRP11	PRP10	-
6th Parameter	1	↑	1	-	-	-	-	-	PRP33	PRP32	PRP31	PRP30	
7th Parameter	1	↑	1	-	-	-	-	PRP44	PRP43	PRP42	PRP41	PRP40	
8th Parameter	1	↑	1	-	VRP13	VRP12	VRP11	VRP10	VRP03	VRP02	VRP01	VRP00	

NOTE: “-” Don’t care, can be set to VDDI or DGND level

Description

-Define by Driver IC Vender but it should be meet 2-type LC requirement

-When turn ON the separate RGB gamma function the command is used for **R-gamma** (‘+’polarity) of GC0 correction characteristics setting

-When turn OFF the separate RGB gamma function the command is used for gamma (‘+’ polarity) correction characteristics setting

Restriction

-

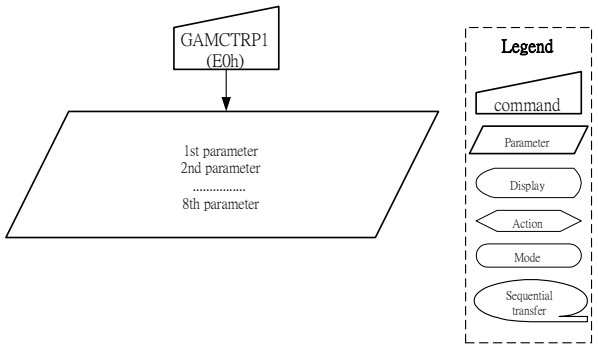
Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Not Fixed
S/W Reset	No Change
H/W Reset	Not Fixed

Flow Chart



6.2.27 GMCTRN0(E1h): Gamma ('-'polarity) Correction Characteristics Setting

E1H	GMCTRN1(Gamma ('-'polarity) Correction Characteristics Setting)												
Inst/ Para	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GMCTRN0	0	↑	1	-	1	1	1	1	0	0	0	1	(E1h)
1st Parameter	1	↑	1	-	-	PKN12	PKN11	PKN10	-	PKN02	PKN01	PKN00	
2nd Parameter	1	↑	1	-	-	PKN32	PKN31	PKN30	-	PKN22	PKN21	PKN20	-
3rd Parameter	1	↑	1	-	-	PKN52	PKN51	PKN50	-	PKN42	PKN41	PKN40	-
4th Parameter	1	↑	1	-	-	-	-	PRN04	PRN03	PRN02	PRN01	PRN00	-
5th Parameter	1	↑	1	-	PRN23	PRN22	PRN21	PRN20	PRN13	PRN12	PRN11	PRN10	-
6th Parameter	1	↑	1	-	-	-	-	-	PRN33	PRN32	PRN31	PRN30	
7th Parameter	1	↑	1	-	-	-	-	PRN44	PRN43	PRN42	PRN41	PRN40	
8th Parameter	1	↑	1	-	VRN13	VRN12	VRN11	VRN10	VRN03	VRN02	VRN01	VRN00	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-Define by Driver IC Vender but it should be meet 2-type LC requirement

-When turn ON the separate RGB gamma function the command is used for **R-gamma** ('-' polarity) of GC0 correction characteristics setting

-When turn OFF the separate RGB gamma function the command is used for GC0 gamma ('-' polarity) correction characteristics setting

Restriction

-

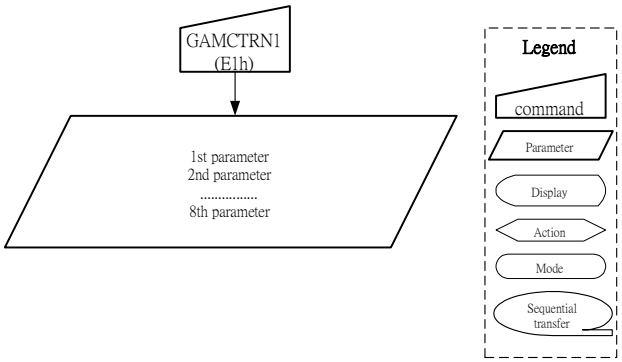
Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Not Fixed
S/W Reset	No Change
H/W Reset	Not Fixed

Flow Chart



6.2.28 GMCTRP2(E2h): Gamma (‘+’polarity) Correction Characteristics Setting

E2H	GMCTRP2 (Gamma (‘+’polarity) Correction Characteristics Setting)												
Inst/ Para	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GMCTRP1	0	↑	1	-	1	1	1	1	0	0	0	0	(E2h)
1st Parameter	1	↑	1	-	-	PKP12	PKP11	PKP10	-	PKP02	PKP01	PKP00	
2nd Parameter	1	↑	1	-	-	PKP32	PKP31	PKP30	-	PKP22	PKP21	PKP20	-
3rd Parameter	1	↑	1	-	-	PKP52	PKP51	PKP50	-	PKP42	PKP41	PKP40	-
4th Parameter	1	↑	1	-	-	-	-	PRP04	PRP03	PRP02	PRP01	PRP00	-
5th Parameter	1	↑	1	-	PRP23	PRP22	PRP21	PRP20	PRP13	PRP12	PRP11	PRP10	-
6th Parameter	1	↑	1	-	-	-	-	-	PRP33	PRP32	PRP31	PRP30	
7th Parameter	1	↑	1	-	-	-	-	PRP44	PRP43	PRP42	PRP41	PRP40	
8th Parameter	1	↑	1	-	VRP13	VRP12	VRP11	VRP10	VRP03	VRP02	VRP01	VRP00	

NOTE: “-” Don’t care, can be set to VDDI or DGND level

Description

-Define by Driver IC Vender but it should be meet 2-type LC requirement

-When turn ON the separate RGB gamma function the command is only used for **G-gamma**

(‘+’polarity) of GC0 correction characteristics setting

-When turn OFF the separate RGB gamma function the command is not used.

Restriction

-

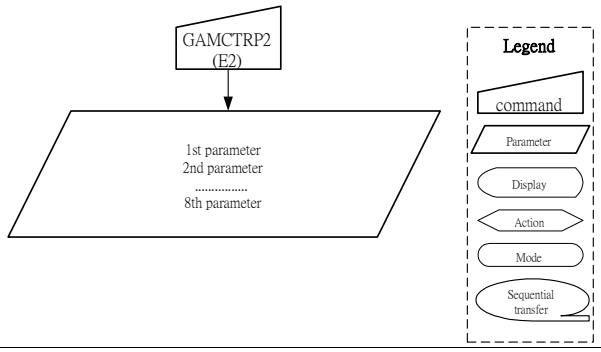
Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Not Fixed
S/W Reset	No Change
H/W Reset	Not Fixed

Flow Chart



6.2.29 GMCTRN2(E3h): Gamma (‘-’polarity) Correction Characteristics Setting

E3H	GMCTRN2(Gamma (‘-’polarity) Correction Characteristics Setting)												
Inst/ Para	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GMCTRN0	0	↑	1	-	1	1	1	1	0	0	0	1	(E3h)
1st Parameter	1	↑	1	-	-	PKN12	PKN11	PKN10	-	PKN02	PKN01	PKN00	
2nd Parameter	1	↑	1	-	-	PKN32	PKN31	PKN30	-	PKN22	PKN21	PKN20	-
3rd Parameter	1	↑	1	-	-	PKN52	PKN51	PKN50	-	PKN42	PKN41	PKN40	-
4th Parameter	1	↑	1	-	-	-	-	PRN04	PRN03	PRN02	PRN01	PRN00	-
5th Parameter	1	↑	1	-	PRN23	PRN22	PRN21	PRN20	PRN13	PRN12	PRN11	PRN10	-
6th Parameter	1	↑	1	-	-	-	-	-	PRN33	PRN32	PRN31	PRN30	
7th Parameter	1	↑	1	-	-	-	-	PRN44	PRN43	PRN42	PRN41	PRN40	
8th Parameter	1	↑	1	-	VRN13	VRN12	VRN11	VRN10	VRN03	VRN02	VRN01	VRN00	

NOTE: “-” Don’t care, can be set to VDDI or DGND level

Description

-Define by Driver IC Vender but it should be meet 2-type LC requirement

-When turn ON the separate RGB gamma function the command is only used for **G-gamma**

(‘-’polarity) of GC0 correction characteristics setting

-When turn OFF the separate RGB gamma function the command is not used.

Restriction

-

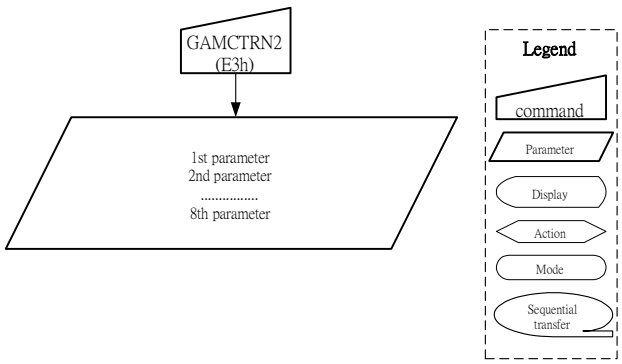
Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Not Fixed
S/W Reset	No Change
H/W Reset	Not Fixed

Flow Chart



6.2.30 GMCTRP3(E4h): Gamma (‘+’polarity) Correction Characteristics Setting

E4H	GMCTRP3 (Gamma (‘+’polarity) Correction Characteristics Setting)												
Inst/ Para	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GMCTRP1	0	↑	1	-	1	1	1	1	0	0	0	0	(E4h)
1st Parameter	1	↑	1	-	-	PKP12	PKP11	PKP10	-	PKP02	PKP01	PKP00	
2nd Parameter	1	↑	1	-	-	PKP32	PKP31	PKP30	-	PKP22	PKP21	PKP20	-
3rd Parameter	1	↑	1	-	-	PKP52	PKP51	PKP50	-	PKP42	PKP41	PKP40	-
4th Parameter	1	↑	1	-	-	-	-	PRP04	PRP03	PRP02	PRP01	PRP00	-
5th Parameter	1	↑	1	-	PRP23	PRP22	PRP21	PRP20	PRP13	PRP12	PRP11	PRP10	-
6th Parameter	1	↑	1	-	-	-	-	-	PRP33	PRP32	PRP31	PRP30	
7th Parameter	1	↑	1	-	-	-	-	PRP44	PRP43	PRP42	PRP41	PRP40	
8th Parameter	1	↑	1	-	VRP13	VRP12	VRP11	VRP10	VRP03	VRP02	VRP01	VRP00	

NOTE: “-” Don’t care, can be set to VDDI or DGND level

Description

-Define by Driver IC Vender but it should be meet 2-type LC requirement

-When turn ON the separate RGB gamma function the command is only used for **B-gamma**

(‘+’polarity) of GC0 correction characteristics setting

-When turn OFF the separate RGB gamma function the command is not used.

Restriction

-

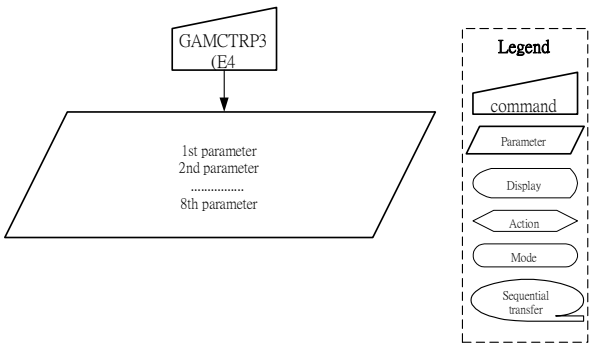
Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Not Fixed
S/W Reset	No Change
H/W Reset	Not Fixed

Flow Chart



6.2.31 GMCTRN3(E5h): Gamma ('-'polarity) Correction Characteristics Setting

E5H	GMCTRN3(Gamma ('-'polarity) Correction Characteristics Setting)												
Inst/ Para	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GMCTRN0	0	↑	1	-	1	1	1	1	0	0	0	1	(E5h)
1st Parameter	1	↑	1	-	-	PKN12	PKN11	PKN10	-	PKN02	PKN01	PKN00	
2nd Parameter	1	↑	1	-	-	PKN32	PKN31	PKN30	-	PKN22	PKN21	PKN20	-
3rd Parameter	1	↑	1	-	-	PKN52	PKN51	PKN50	-	PKN42	PKN41	PKN40	-
4th Parameter	1	↑	1	-	-	-	-	PRN04	PRN03	PRN02	PRN01	PRN00	-
5th Parameter	1	↑	1	-	PRN23	PRN22	PRN21	PRN20	PRN13	PRN12	PRN11	PRN10	-
6th Parameter	1	↑	1	-	-	-	-	-	PRN33	PRN32	PRN31	PRN30	
7th Parameter	1	↑	1	-	-	-	-	PRN44	PRN43	PRN42	PRN41	PRN40	
8th Parameter	1	↑	1	-	VRN13	VRN12	VRN11	VRN10	VRN03	VRN02	VRN01	VRN00	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-Define by Driver IC Vender but it should be meet 2-type LC requirement

-When turn ON the separate RGB gamma function the command is only used for **B-gamma** ('-' polarity) of GC0 correction characteristics setting

-When turn OFF the separate RGB gamma function the command is not used.

Restriction

-

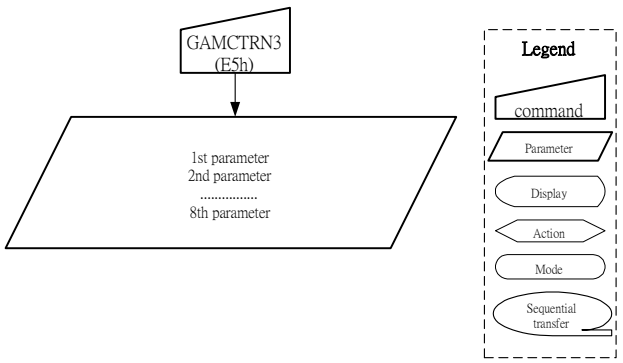
Register Available

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Not Fixed
S/W Reset	No Change
H/W Reset	Not Fixed

Flow Chart



6.2.32 GAM_R_SEL: Gamma selection (F2h)

F2H	Gamma selection (GAMCTRL)												
Inst/ Para	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GAMCTRL	0	↑	1	-	1	1	0	1	1	1	1	GAM_R_SEL	(F2h)

NOTE: "-" Don't care

Description	**GAM_R_SEL:** Gamma selection 0: Gamma control by RE0 & RE1 registers value. 1: Gamma control by GC0~GC3 ROM value. (Cooperate with R26h register) D0: The flag must be fixed at 0. D2: The flag must be fixed at 1. D3: The flag must be fixed at 1.
Restriction	-
Register Available	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status / Default Value (GAM_R_SEL) Power On Sequence: 0 S/W Reset: 0 H/W Reset: 0
Flow Chart	

6.3 Reset Table (Default Value)

GM=00,176RGBX220

Item	Register	After	After Hardware	After Software Reset
Frame memory		Random	No Change	No Change
Sleep In/Out	**10h/ 11h**	In	In	In
Display On/Off	**29h/ 28h**	Off	Off	Off
Display mode	**13h/ 12h**	Normal	Normal	Normal
Display Inversion On/Off	**21h/ 20h**	Off	Off	Off
Display Idle Mode On/Off	**39h/ 38h**	Off	Off	Off
Column: Start Address (XS)	**2Ah**	0000h	0000h	0000h
Column: End Address (XE)	**2Ah**	00AFh	00AFh	00AFh (when MV=0) 00DBh (when MV=1)
Row: Start Address (YS)	**2Bh**	0000h	0000h	0000h
Row: End Address (YE)	**2Bh**	00DBh	00DBh	00DBh (when MV=0) 00AFh (when MV=1)
RGB for 4k, 65k, 262K Color	**2Dh**	Random	See Section	No Change
Partial: Start Address (PSL)	**30h**	0000h	0000h	0000h
Partial: End Address (PEL)	**30h**	00DBh	00DBh	00DBh
Scroll: Vertical scrolling		Off	Off	Off
Scroll: Top Fixed Area	**33h**	0000h	0000h	0000h
Scroll: Scroll Area (VSA)	**33h**	00DCh	00DCh	00DCh
Scroll: Bottom Fixed Area	**33h**	0000h	0000h	0000h
Scroll Start Address (SSA)	**37h**	0000h	0000h	0000h
Tearing: On/Off	**35h/ 34h**	Off	Off	Off
Tearing Effect Mode *3)	**35h**	00h	00h (Mode1)	00h (Mode1)
Memory Data Access	**36h**	0/0/0/0/0	0/0/0/0/0	No Change
Interface Pixel Color	**3Ah**	56h	56h	No Change
RDDPM	**0Ah**	08h	08h	08h
RDDMADCTR	**0Bh**	00h	00h	No Change
RDDCOLMOD	**0Ch**	56h	56h	No Change
RDDIM	**0Dh**	00h	00h	00h
RDDSM	**0Eh**	00h	00h	00h
RDDSDR	**0Fh**	00h	00h	00h
ID1	**DAh**	38h	38h	38h
ID2	**DBh**	8xh	8xh	8xh
ID3	**DCh**	62h	62h	62h

Notes 1. There will be no abnormal visible effects on the display when S/W or H/W Reset is applied. Notes:2. Powered-On Reset finishes within 10μs after both VDD & VDDI are applied.

Notes:3. TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

GM=01,176RGBX176

Item	Register	After	After Hardware	After Software Reset
Frame memory		Random	No Change	No Change
Sleep In/Out	**10h/ 11h**	In	In	In
Display On/Off	**29h/ 28h**	Off	Off	Off
Display mode	**13h/ 12h**	Normal	Normal	Normal
Display Inversion On/Off	**21h/ 20h**	Off	Off	Off
Display Idle Mode On/Off	**39h/ 38h**	Off	Off	Off
Column: Start Address (XS)	**2Ah**	0000h	0000h	0000h
Column: End Address (XE)	**2Ah**	00AFh	00AFh	00AFh (when MV=0) 00AFh (when MV=1)
Row: Start Address (YS)	**2Bh**	0000h	0000h	0000h
Row: End Address (YE)	**2Bh**	00AFh	00AFh	00AFh (when MV=0) 00AFh (when MV=1)
RGB for 4k, 65k, 262K Color	**2Dh**	Random	See Section	No Change
Partial: Start Address (PSL)	**30h**	0000h	0000h	0000h
Partial: End Address (PEL)	**30h**	00AFh	00AFh	00AFh
Scroll: Vertical scrolling		Off	Off	Off
Scroll: Top Fixed Area	**33h**	0000h	0000h	0000h
Scroll: Scroll Area (VSA)	**33h**	00B0h	00B0h	00B0h
Scroll: Bottom Fixed Area	**33h**	0000h	0000h	0000h
Scroll Start Address (SSA)	**37h**	0000h	0000h	0000h
Tearing: On/Off	**35h/ 34h**	Off	Off	Off
Tearing Effect Mode *3)	**35h**	00h	00h (Mode1)	00h (Mode1)
Memory Data Access	**36h**	0/0/0/0/0	0/0/0/0/0	No Change
Interface Pixel Color	**3Ah**	56h	56h	No Change
RDDPM	**0Ah**	08h	08h	08h
RDDMADCTR	**0Bh**	00h	00h	No Change
RDDCOLMOD	**0Ch**	56h	56h	No Change
RDDIM	**0Dh**	00h	00h	00h
RDDSM	**0Eh**	00h	00h	00h
RDDSDR	**0Fh**	00h	00h	00h
ID1	**DAh**	38h	38h	38h
ID2	**DBh**	8xh	8xh	8xh
ID3	**DCh**	62h	62h	62h

Notes 1. There will be no abnormal visible effects on the display when S/W or H/W Reset is applied. Notes:2. Powered-On Reset finishes within 10μs after both VDD & VDDI are applied.

Notes:3. TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

GM=11,176RGBX132

Item	Register	After	After Hardware	After Software Reset
Frame memory		Random	No Change	No Change
Sleep In/Out	**10h/ 11h**	In	In	In
Display On/Off	**29h/ 28h**	Off	Off	Off
Display mode	**13h/ 12h**	Normal	Normal	Normal
Display Inversion On/Off	**21h/ 20h**	Off	Off	Off
Display Idle Mode On/Off	**39h/ 38h**	Off	Off	Off
Column: Start Address (XS)	**2Ah**	0000h	0000h	0000h
Column: End Address (XE)	**2Ah**	00AFh	00AFh	00AFh (when MV=0) 0083h (when MV=1)
Row: Start Address (YS)	**2Bh**	0000h	0000h	0000h
Row: End Address (YE)	**2Bh**	0083h	0083h	0083h (when MV=0) 00AFh (when MV=1)
RGB for 4k, 65k, 262K Color	**2Dh**	Random	See Section	No Change
Partial: Start Address (PSL)	**30h**	0000h	0000h	0000h
Partial: End Address (PEL)	**30h**	0083h	0083h	0083h
Scroll: Vertical scrolling		Off	Off	Off
Scroll: Top Fixed Area	**33h**	0000h	0000h	0000h
Scroll: Scroll Area (VSA)	**33h**	0084h	0084h	0084h
Scroll: Bottom Fixed Area	**33h**	0000h	0000h	0000h
Scroll Start Address (SSA)	**37h**	0000h	0000h	0000h
Tearing: On/Off	**35h/ 34h**	Off	Off	Off
Tearing Effect Mode *3)	**35h**	00h	00h (Mode1)	00h (Mode1)
Memory Data Access	**36h**	0/0/0/0/0	0/0/0/0/0	No Change
Interface Pixel Color	**3Ah**	56h	56h	No Change
RDDPM	**0Ah**	08h	08h	08h
RDDMADCTR	**0Bh**	00h	00h	No Change
RDDCOLMOD	**0Ch**	56h	56h	No Change
RDDIM	**0Dh**	00h	00h	00h
RDDSM	**0Eh**	00h	00h	00h
RDDSDR	**0Fh**	00h	00h	00h
ID1	**DAh**	38h	38h	38h
ID2	**DBh**	8xh	8xh	8xh
ID3	**DCh**	62h	62h	62h

Notes 1. There will be no abnormal visible effects on the display when S/W or H/W Reset is applied. Notes:2. Powered-On Reset finishes within 10μs after both VDD & VDDI are applied.

Notes:3. TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

7 DRIVER ELECTRICAL CHARACTERISTIC

7.1. Absolute Maximum Ratings

Table 7.1: Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	VDD	-0.3 ~ +4.6	V
Supply voltage (Logic)	VDDI	-0.3 ~ +4.6	V
Supply voltage (Digital)	VCC	-0.3 ~ +2.4	V
Driver supply Voltage	VGH-VGL	-0.3 ~ +33.0	V
Logic Input voltage range	V IN	-0.3 ~ VDDI + 0.3	V
Logic Output voltage range	VO	-0.3 ~ VDDI + 0.3	V
Operating temperature range	TOPR	-40 ~ +85	℃
Storage Temperature range	TSTG	-55 ~ +125	℃

Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

7.2 ESD Protection Level

Table 7.2: ESD Protection Level

Model	Test Condition	Protection Level	Unit
ESD Human Body Model	C = 100 pF, R = 1.5 kΩ 3 times zapping/ each pin, 1sec/ a zapping	±2500 for each pin ±3000 for connecter pin	V
ESD Machine Model	C = 200 pF, R = 0.0 Ω 3 times zapping/ each pin, 1sec/a zapping	±250 for each pin	V

Note: connecter pin is DATA BUS, Power, CSX, RDX, WRX, RESX, TE

7.3 LATCH-UP PROTECTION LEVEL

The device will not latch up at trigger current levels less than ± 100 mA.

7.4 Light Sensitivity

The operation of the IC will not be materially altered by incident light.

7.5 DC Characteristics

Table 7.5: Interface DC Characteristics

Parameter	Symbol	Conditions	Specification TYP			Unit	Related Pins
			MIN	TYP	MAX		
Power & Operation Voltage							
Analog Operating voltage	VDD	Operating Voltage	2.6	3.0	3.5	V	Note 2
Logic Operating voltage	VDDI	I/O supply voltage	1.6	3.3	3.5	V	Note 2
Digital Operating voltage	VCC	Digital supply voltage	1.5	1.8	2.0	V	Note 2
Gate Driver High voltage	VGH		10.0		16.5	V	Note 3
Gate Driver Low voltage	VGL		-16.75		-9.0	V	Note 3
Driver Supply voltage		|VGH-VGL|	19		33.25	V	Note 3
Input /Output							
Logic High level input voltage	VIH		0.7VDDI	-	VDDI	V	Note 1, 2, 3
Logic Low level input voltage	VIL	-	VSS	-	0.3VDDI	V	Note 1, 2, 3
Logic High level output voltage	VOH	IOH = -1.0mA	0.8VDDI	-	VDDI	V	Note 1, 2, 3
Logic Low level output voltage	VOL	IOL = 1.0mA	VSS	-	0.2VDDI	V	Note 1, 2, 3
Logic High level input current	IIH				1	μA	Note 1, 2, 3
Logic Low level input current	IIL		-1			μA	Note 1, 2, 3
Logic Input leakage current	IIL	VIN = VDDI or VSS	-0.1	-	+0.1	μA	Note 1, 2, 3
VCOM Operation							
VCOM High voltage	VCOMH	Ccom=12nF	2.5		5.0	V	Note 3
VCOM Low voltage	VCOML	Ccom=12nF	-2.5		0.0	V	Note 3
VCOM Amplitude voltage	VCOMA	|VCOMH-VCOML|	4.0		5.5	V	Note 3
Source Driver							
Source output range	VSout		0.1		AVDD-0.1	V	Note 4
Gamma reference voltage	GVDD		3.0		5.0	V	Note 3
Source output settling time	Tr	Below with 99% precision	20		25	μs	Note 4, 5 Fig.6.5.2
Output deviation voltage (Source output channel)	V,dev	Sout >= 4.2V, Sout <= 0.8V			20	mV	Note 4 Fig.6.5.3
		4.2V>Sout>0.8V			6	mV	
Output offset voltage	VOFSET				35	mV	Note 8
Booster Operation							
1st Booster (VDDx2) voltage	AVDD		4.95 *6)		5.5 *7)	V	Note 3
1st Booster (VDDx2) Drop voltage	VDDx2,drop	I loading = 1mA			5	%	Note 3
Linear range	VLinear		0.2		AVDD-0.2	V	

Note 1: VDDI=1.6 to 3.5V, VDD=2.6 to 3.5V, AGND=DGND=0V, Ta=-30 to 70 ℃ (to +85℃ no damage)

Note 2, 3, 4: When the measurements are performed with LCD module, Measurement Points are like below.

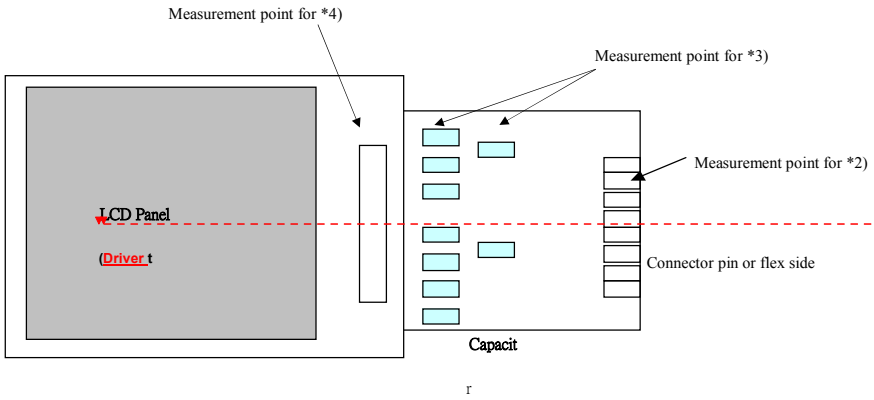
Note 3: CSX, RDX, WRX, D[23:0], D/CX, RESX, TE, PCLK, VS, HS, DE, SDA, SCL, GM1, GM0, LCM, RCM1, RCM0, P68, IM2, IM1, IM0, SRGB, REV, SMX, SMY, RL, TB, IDM, SHUT and Test pins

Note 5, Source channel loading= 10pF/channel, Gate channel loading= 50pF/channel.

Note 6, VDD=2.6V or VCI1=2.6V

Note 7, VDD=3.0V or VCI1=3.0V

Note 8, The Max. value is between with Note 4 measure point and Gamma setting value.



删除: MCU

删除: r

Fig 7.5.1 Measurement Points for All Characteristics.

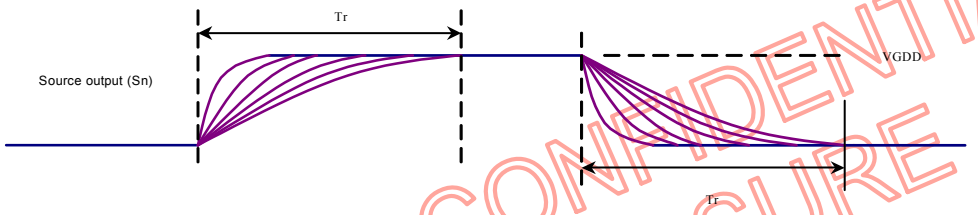


Fig. 7.5.2 Tr : Source output stable timing

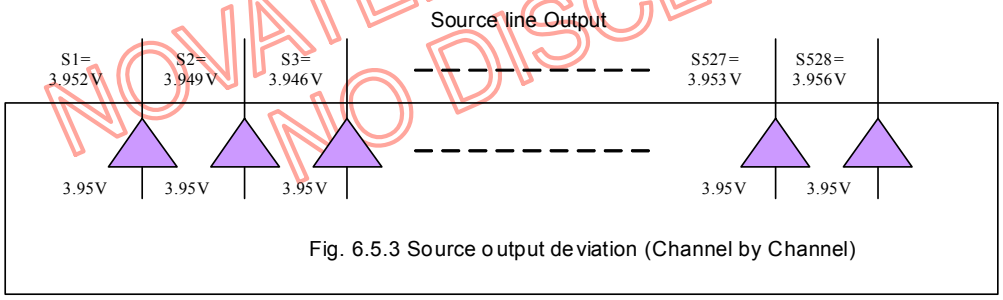


Fig. 6.5.3 Source output deviation (Channel by Channel)

-When Sout >=4.2V, Sout<=0.8V

Max (S1, S2, S3, …. , S528) – Min (S1, S2, S3, …. , S528) <= 20mV

-When 4.2V>Sout>0.8V

Max (S1, S2, S3, …. , S528) – Min (S1, S2, S3, …. , S528) <= 6mV

-Example

When Sout level is 3.95V (Gray scale voltage) Max (S1, S2, S3, …. , S528) = 3.956V Min (S1, S2, S3, …. , S528) = 3.946V Sout deviation =

Max (S1, S2, S3, …. , S528) – Min (S1, S2, S3, …. , S528) = 10mV <- Out Spec

7.6 Power Consumption (TBD)

Note: Power consumption table is included display module specification.

Mode of operation	Frame Frequency	Inversion Mode	Image	B5; B6; B7	Current consumption					
					Typical		Maximum		Worst case	
					IDDI (mA)	IDD (mA)	IDDI (mA)	IDD (mA)	IDDI (mA)	IDD (mA)
-Normal Mode On -Partial Mode Off -Idle Mode Off -Sleep Out Mode (6)	60Hz ±10 %	One Line	Note 1	X;X;X						
		One Line	Note 2	X;X;X						
		One Line	Note 3	X;X;X						
		One Line	Note 4	X;X;X						
		One Line	Note 5	X;X;X						
		One Line	Note 8	X;X;X						
-Normal Mode On -Partial Mode Off -Idle Mode On -Sleep Out Mode (6)	60Hz ±10 %	One Line	Note 5	X;X;X						
-Normal Mode Off -Partial Mode On -(40 lines) -Idle Mode Off -Sleep Out Mode(6	60Hz ±10 %	One Line	Gray Levels	X;X;X						
-Normal Mode Off -Partial Mode On -(40 lines) -Idle Mode On -Sleep Out Mode (6)	60Hz ±10 %	One Line	Note 7	X;X;X						
		One Line	Note 7	X;X;X						
-Sleep In Mode (6)	N/A	N/A	N/A	X;X;X						
-Normal Mode On -Partial Mode Off -Idle Mode Off -Sleep Out Mode	60Hz ±10 %	One Line	262k Colors Note 9 CPU Access @ 15 fps	0;0;0						
				0;0;1						
				0;1;0						
				0;1;1						
				1;0;0						
				1;0;1						
				1;1;0						
				1;1;1						
			262k Colors Note 9 CPU Access @ 25 fps	0;0;0						
				0;0;1						
				0;1;0						
				0;1;1						
				1;0;0						
				1;0;1						
				1;1;0						
				1;1;1						

Table 7.6 Power consumption of display module, Architecture type I

Notes:

1. All pixels black.

2. All pixels white.

3. Checker board 4 by 4.

4. Grayscale from top to bottom.

5. 20 % Black, 80 % White.

6. CPU access is inactive.

7. Black & White Checker board 8 by 8.

8. Absolute Worst Case Patterns: All pixels black.

9. Absolute Worst Case Patterns and Sequences: It depends on driver construction.

10. Absolute worst case of VDD current is less than TBD mA in the case of CPU access is inactive, Normal Mode On, Partial Mode Off, Idle Mode Off, Sleep Out mode.

11. Absolute worst case of VDDI current is less than TBD mA in the case of CPU access is inactive, Normal Mode On, Partial Mode Off, Idle Mode Off, Sleep Out mode.

12. Inrush currents are not included in current consumption values.

Typical Case:
T_A = 25 °C
VDD = 2.78 V
VDDI = 1.80 V

Worst Case:
T_A = -30 to70 °C
VDD = 2.60 V to 3.5 V
VDDI = 1.60 V to 3.5 V
Includes Process Variance.

7.7 AC CHARACTERISTICS

7.7.1 Parallel Interface Characteristics 18, 16, 9 or 8-bits bus (8080-series MCU)

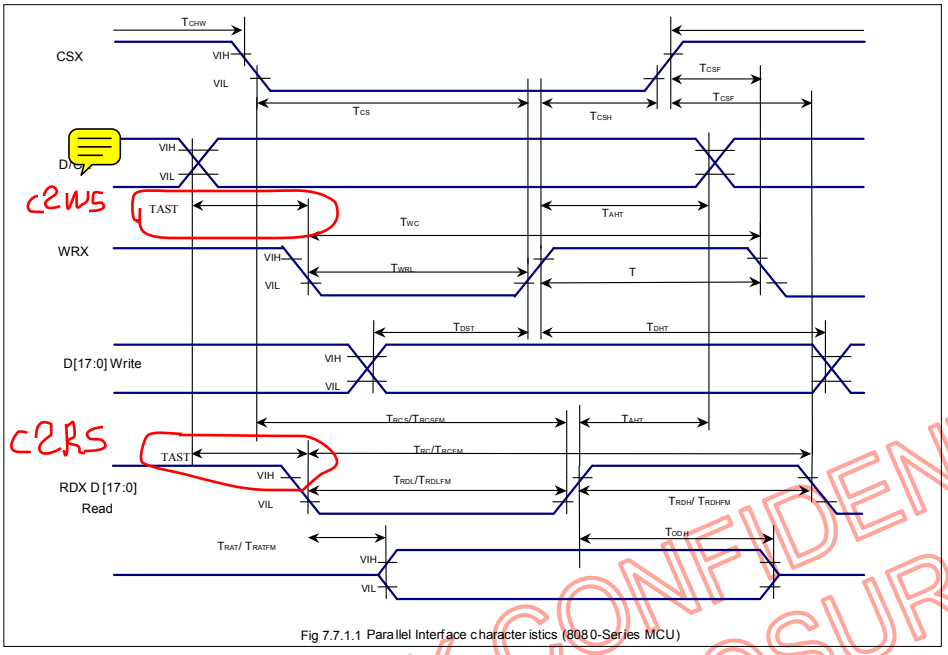


Fig 7.7.1.1 Parallel Interface characteristics (8080-Series MCU)

Table .7.7.1: AC Characteristics for Parallel Interface 24, 16, 8-bits bus (8080-series MCU)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
D/CX	tAST	Address setup time	10		ns	-
	tAHT	Address hold time (Write/Read)	10		ns	
CSX	tCHW	Chip select “H”pulse width	0		ns	
	tCS	Chip select setup time (Write)	35		ns	
	tRCS	Chip select setup time (Read ID)	45		ns	
	tRCSFM	Chip select setup time (Read FM)	355		ns	
	tCSF	Chip select wait time (Write/Read)	10		ns	
	tCSH	Chip select hold time	2		ns	
WRX	tWC	Write cycle	100		ns	
	tWRH	Control pulse “H” duration	35		ns	
	tWRL	Control pulse “L” duration	35		ns	
RDX (ID)	tRC	Read cycle (ID)	160		ns	When read ID data
	tRDH	Control pulse “H” duration (ID)	90		ns	
	tRDL	Control pulse “L” duration (ID)	45		ns	
RDX (FM)	tRCFM	Read cycle (FM)	450		ns	When read from frame memory
	tRDHFM	Control pulse “H” duration (FM)	90		ns	
	tRDLFM	Control pulse “L” duration (FM)	355		ns	
D[17:0]	tDST	Data setup time	10		ns	For maximum CL=30pF For minimum CL=8pF
	tDHT	Data hold time	10		ns	
	tRAT	Read access time (ID)		40	ns	
	tRATFM	Read access time (FM)		340	ns	
	tODH	Output disable time	20	80	ns	

Note 1: VDDI=1.6 to 3.5V, VDD=2.6 to 3.5V, AGND=DGND=0V, Ta=-30 to 70℃ (to +85℃ no damage)

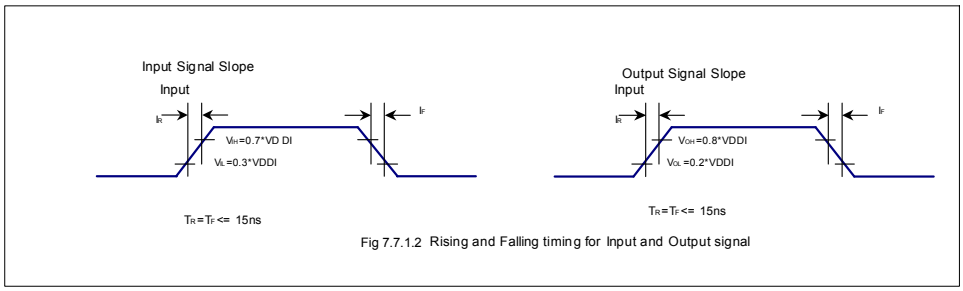


Fig 7.7.1.2 Rising and Falling timing for Input and Output signal

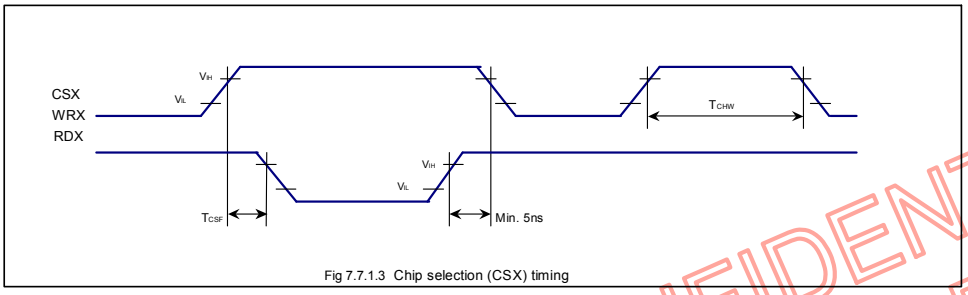


Fig 7.7.1.3 Chip selection (CSX) timing

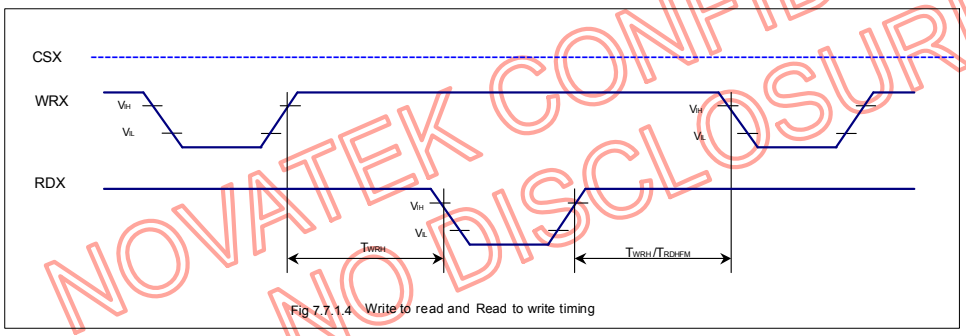


Fig 7.7.1.4 Write to read and Read to write timing

NOTE: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.7.2 Parallel Interface Characteristics 18, 16, 9 or 8-bits bus (6800-series MCU)

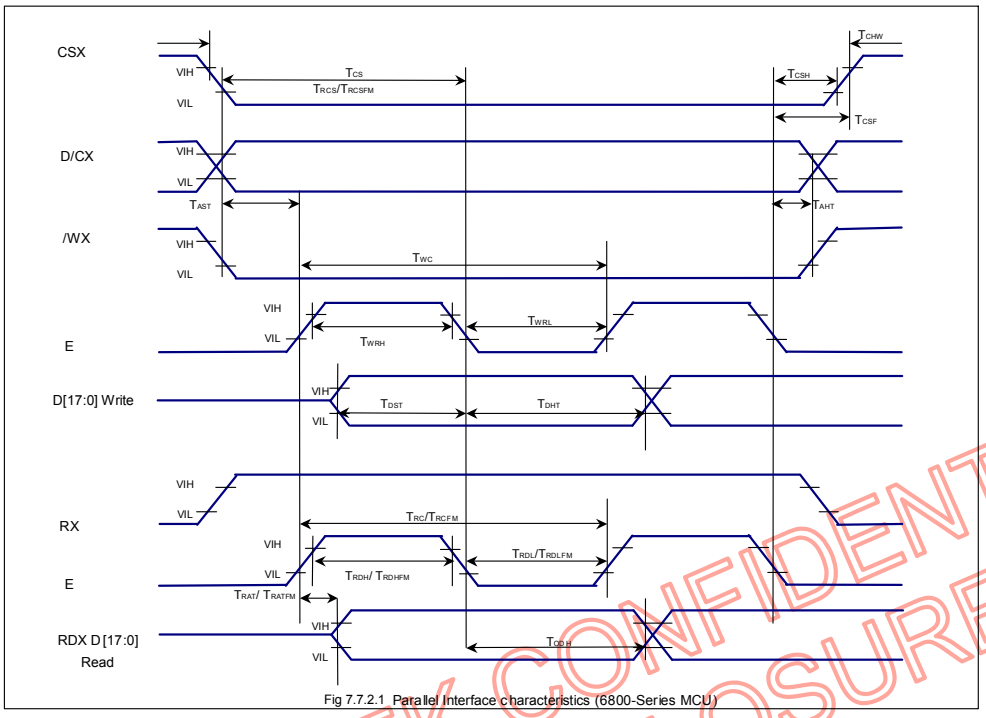


Fig 7.7.2.1 Parallel Interface characteristics (6800-Series MCU)

Table 7.7.2: AC Characteristics for Parallel Interface 24, 16, 8-bits bus (6800-series MCU)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
D/CX	tAST	Address setup time	10		ns	-
	tAHT	Address hold time (Write/Read)	10		ns	
CSX	tCHW	Chip select “H” pulse width	0		ns	-
	tCS	Chip select setup time (Write)	35		ns	
	tRCS	Chip select setup time (Read ID)	45		ns	
	tRCSFM	Chip select setup time (Read FM)	355		ns	
	tCSF	Chip select wait time (Write/Read)	10		ns	
	tCSH	Chip select hold time	10		ns	
WRX	tWC	Write cycle	100		ns	
	tWRH	Control pulse “H” duration	35		ns	
	tWRL	Control pulse “L” duration	35		ns	
RDX (ID)	tRC	Read cycle (ID)	160		ns	When read ID data
	tRDH	Control pulse “H” duration (ID)	90		ns	
	tRDL	Control pulse “L” duration (ID)	45		ns	
RDX (FM)	tRCFM	Read cycle (FM)	450		ns	When read from frame memory
	tRDHFM	Control pulse “H” duration (FM)	90		ns	
	tRDLFM	Control pulse “L” duration (FM)	355		ns	
D[17:0]	tDST	Data setup time	10		ns	For maximum CL=30pF For minimum CL=8pF
	tDHT	Data hold time	10		ns	
	tRAT	Read access time (ID)		40	ns	
	tRATFM	Read access time (FM)		340	ns	
	tODH	Output disable time	20	80	ns	

Note 1: VDDI=1.6 to 3.5V, VDD=2.6 to 3.5V, AGND=DGND=0V, Ta=-30 to 70℃ (to +85℃ no damage)

Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

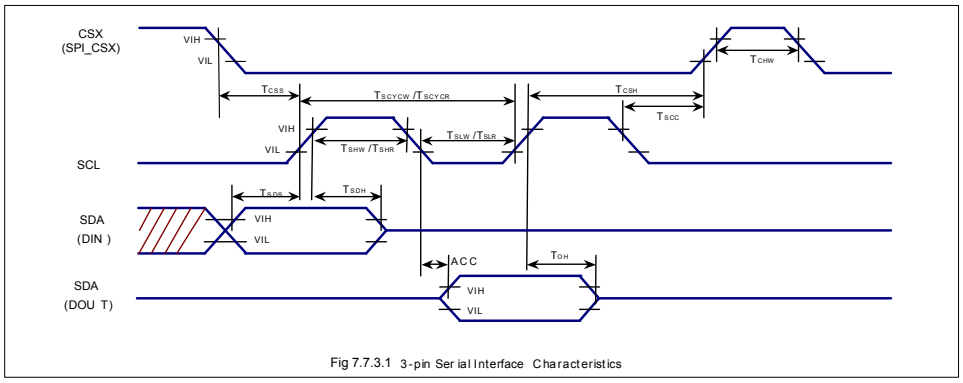


Fig 7.7.3.1 3-pin Serial Interface Characteristics

7.7.3 Serial Interface Characteristics (3-pin Serial)

Table 7.7.3: 3-pin Serial Interface Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	tCSS	Chip select setup time	60		ns	
	tCSH	Chip select hold time	65		ns	
	tSCC	Chip select setup time	20		ns	
	tCHW	Chip select setup time	40		ns	
SCL	tSCYCW	Serial clock cycle (Write)	65		ns	-
	tSCYCR	Serial clock cycle (Read)	1		us	
	tSHW	SCL “H” pulse width (Write)	35		ns	
	tSHR	SCL “H” pulse width (Read)	450		ns	
	tSLW	SCL “L” pulse width (Write)	35		ns	
	tSLR	SCL “L” pulse width (Read)	450		ns	
	tSCYCR	Serial clock cycle (Read ID)	150		ns	
	tSHR	SCL “H” pulse width (Read ID)	60		ns	
	tSLR	SCL “L” pulse width (Read ID)	60		ns	
SDA (DIN) (DOUT)	tSDS	Data setup time	30		ns	
	tSDH	Data hold time	30		ns	
	tACC	Access time	10		ns	For maximum L=30pF
	tOH	Output disable time	15		ns	For minimum CL=8pF

Note 1: VDDI=1.6 to 3.5V, VDD=2.6 to 3.5V, AGND=DGND=0V, Ta=-30 to 70℃ (to +85℃ no damage)
Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.7.4 RGB Interface Characteristics

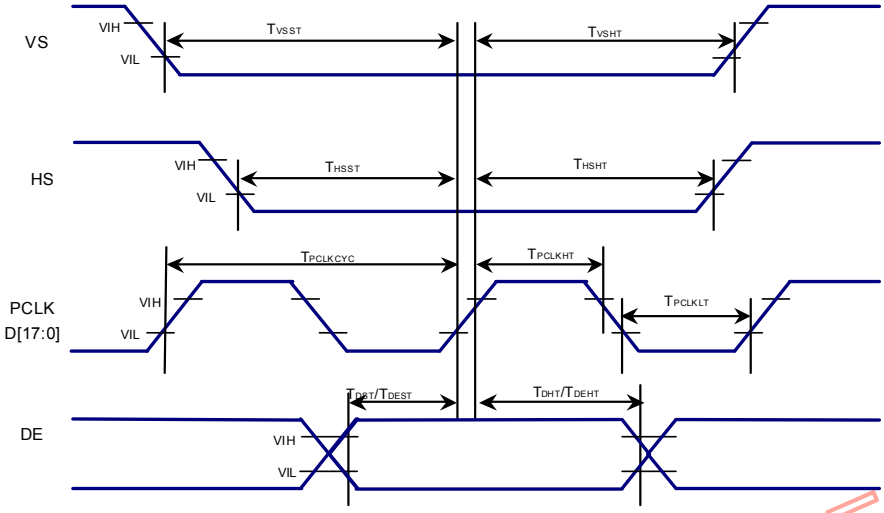


Fig 7.7.4 General Timing for RGB I/F

Table 7.7.4 General Timing for RGB I/F

Item	Symbol	Condition	Specification			Unit
			Min	Type.	Max	
Pixel low pulse width	TPCLKLT		15			ns
Pixel high pulse width	TPCLKHT		15			ns
Vertical Sync. set-up time	TVSST		15			ns
Vertical Sync. hold time	TVSSHT		15			ns
Horizontal Sync. set-up time	THSST		15			ns
Horizontal Sync. hold time	TVSSHT		15			ns
Data Enable set-up time	TDEST		15			ns
Data Enable hold time	TDEHT		15			ns
Data set-up time	TDST		15			ns
Data hold time	TDHT		15			ns

Note 1: VDDI=1.6 to 3.5V, VDD=2.6 to 3.5V, AGND=DGND=0V, Ta=-30 to 70℃ (to +85℃ no damage)

Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Note 3. Data lines can be set to "High" or "Low" during blanking time_ Don't care.

Note 4. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Note 5. HP is multiples of eight PCLK.

7.7.5 Reset Input Timing

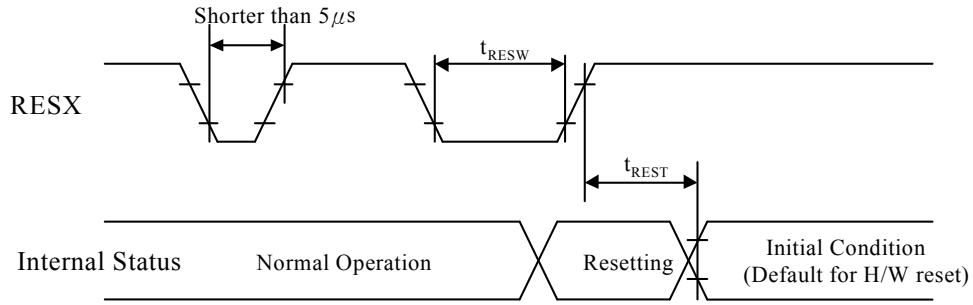


Table 7.7.5 Reset input timing

(V_{SS}=0V, VDDI=1.65V to 1.95V, VDD=2.6V to 2.9V,Ta = -30 to 70° C)

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
tRESW	*1) Reset low pulse width	RESX	10	-	-	-	μs
tREST	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

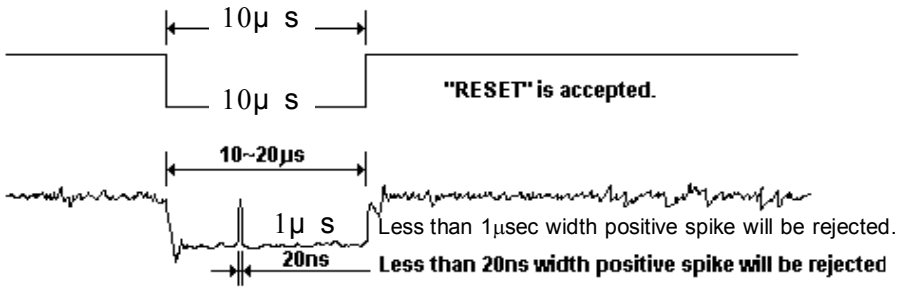
Note 1 Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 10μs	Reset
Between 5μs and 10μs	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, ID2 and VCOMOF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:

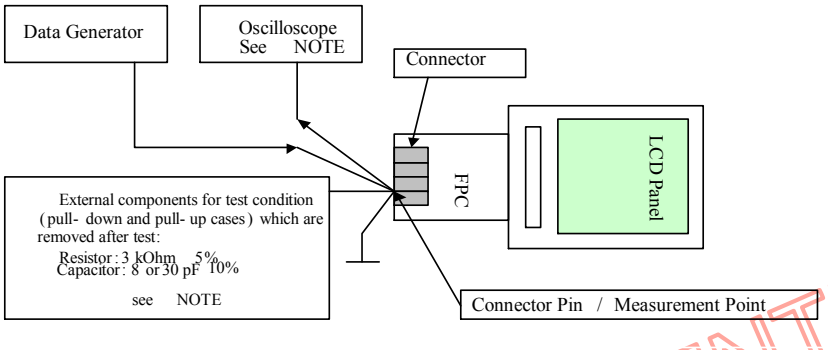


Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.7.6.1 Parallel Interface Characteristics 24, 18, 16 or 8-bits bus (8080 & 6800-series MCU)

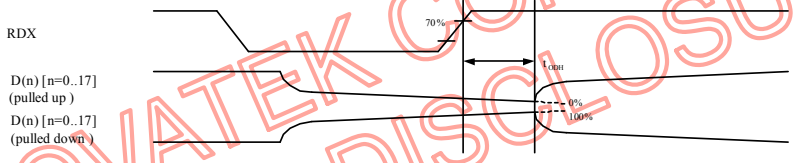
tRAT, tRATFM, tODH Measurement Condition:

Measurement Condition Set-up

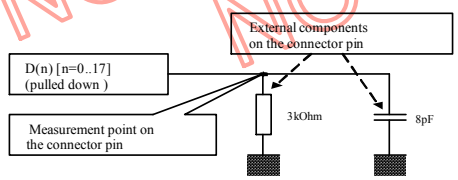


Note: Capacitances and resistances of the oscilloscope's probe must be included externals components in these measurements.

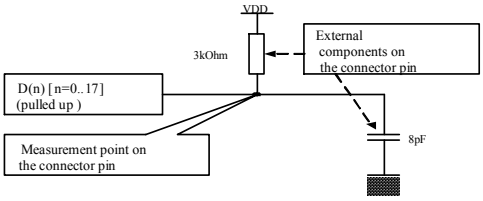
Minimum Value Measurement



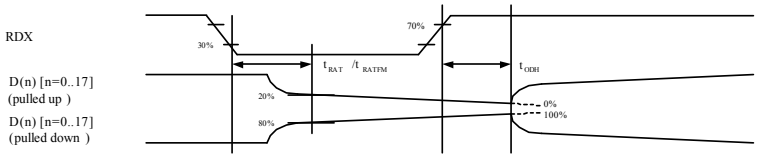
Measurement circuit pulled down



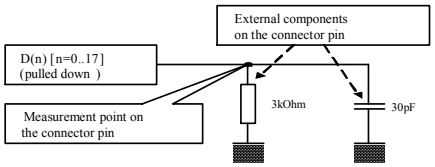
Measurement circuit pulled up



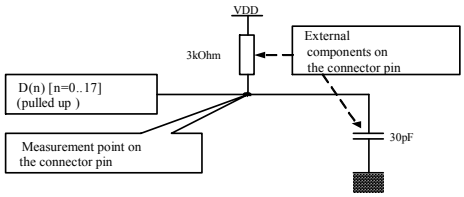
Maximum Value Measurement



Measurement circuit pulled down



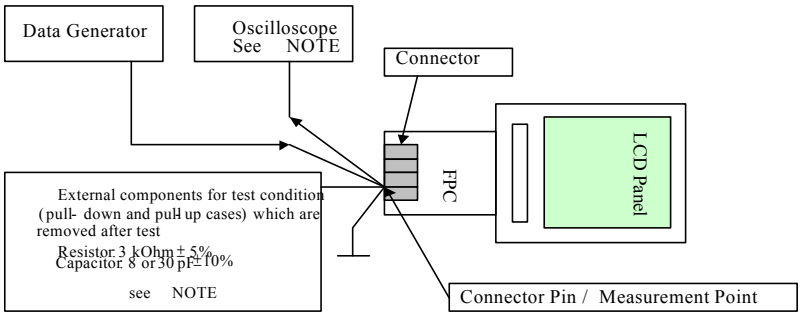
Measurement circuit pulled up



7.7.6.2 Serial Interface Characteristics

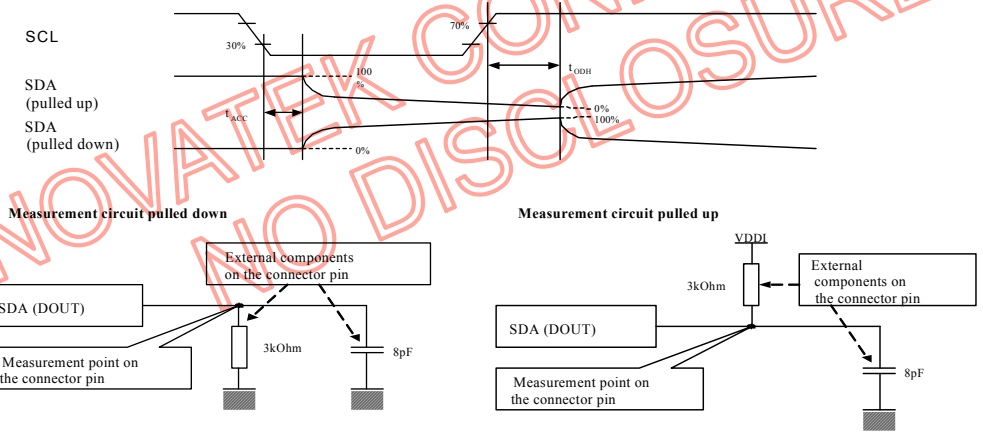
tACC, tOH Measurement Condition

Measurement Condition Set-up



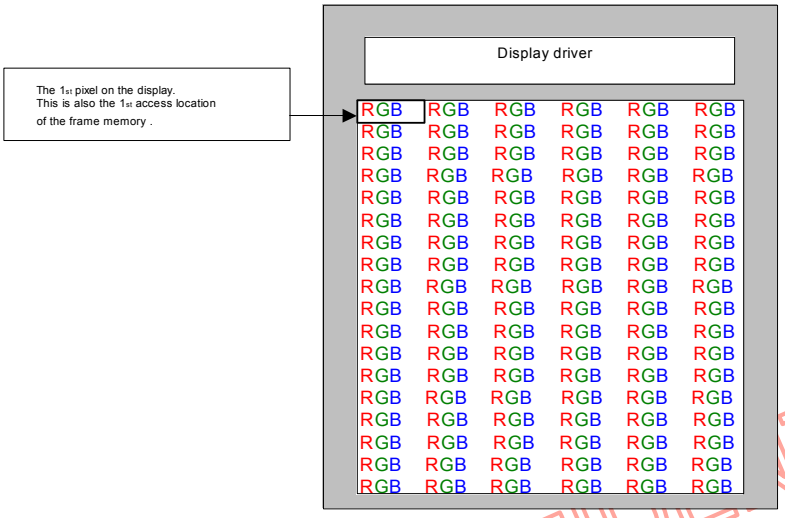
Note: Capacitances and resistances of the oscilloscope' s probe must be included externals components in these measurements.

Minimum Value Measurement



8 DISPLAY MODULE DEFAULT PPOSITION

The default position of the display is always as follow, when MADCTR's (36h) parameter is 00h.



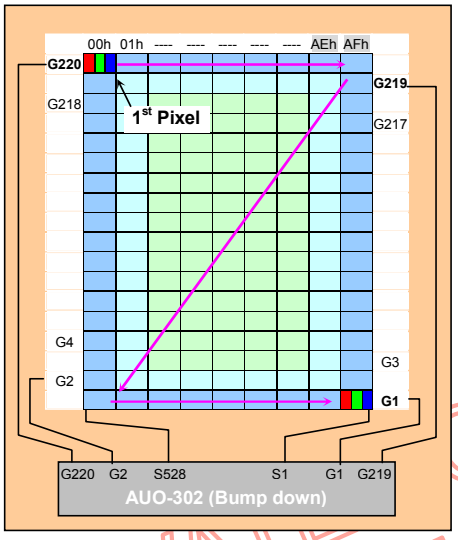
9 EXAMPLE CONNECTION WITH PANEL DIRECTION AND DIFFERENT RESOLUTION

9.1 Application of connection with panel direction

Case 1:

- 1st Pixel is at *Left Top* of the panel & Driver IC on bottom

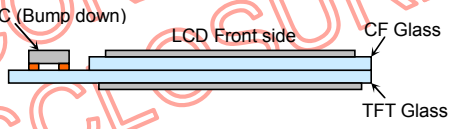
- RGB filter order = RGB



- Direction default setting (H/W)
  SMX = '1' (S528->S1)
  SMY = '1' (G220-G1)
  SRGB = '1'

  S1 = Filter B
  S2 = Filter G
  S3 = Filter R

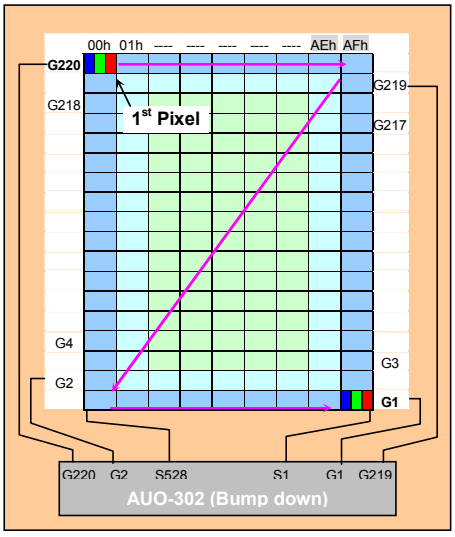
- Display direction control (S/W) (36H)
  - X-Mirror control by MX (D7)
  - Y-Mirror control by MY (D6)
  - XY-Exchange control by MV (D5)



Case 2:

- 1st Pixel is at *Left Top* of the panel

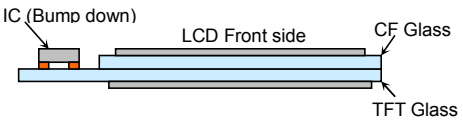
- RGB filter order = BGR



- Direction default setting (H/W)
  SMX = '1' (S528->S1)
  SMY = '1' (G220-G1)
  SRGB = '0'

  S1 = Filter R
  S2 = Filter G
  S3 = Filter B

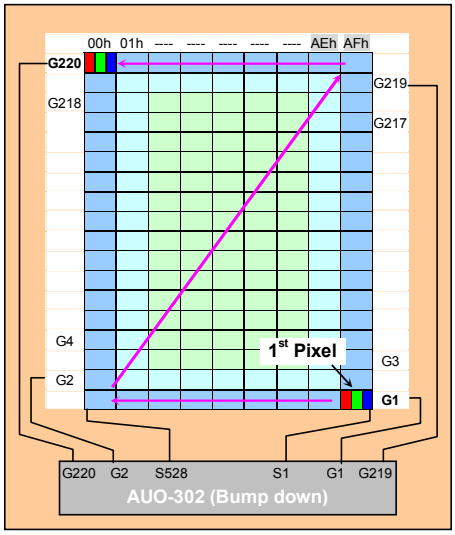
- Display direction control (S/W) (36H)
  - X-Mirror control by MX (D7)
  - Y-Mirror control by MY (D6)
- XY-Exchange control by MV (D5)



Case 3:

- 1st Pixel is at *Righ Bottom* of the panel

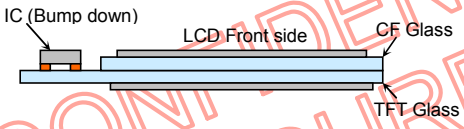
- RGB filter order = RGB



- Direction default setting (H/W)
  SMX = '0' (S1->S528)
  SMY = '0' (G1-G220)
  SRGB = '1'

  S1 = Filter B
  S2 = Filter G
  S3 = Filter R

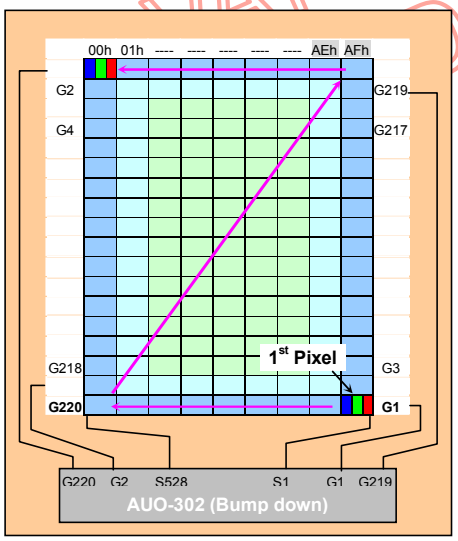
- Display direction control (S/W) (36H)
  - X-Mirror control by MX (D7)
  - Y-Mirror control by MY (D6)
  - XY-Exchange control by MV (D5)



Case 4:

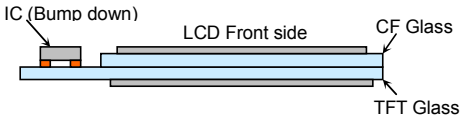
- 1st Pixel is at *Righ Bottom* of the panel

- RGB filter order = BGR



- Direction default setting (H/W)
  SMX = '0' (S1->S528)
  SMY = '0' (G1-G220)
  SRGB = '0'

  S1 = Filter R
  S2 = Filter G
  S3 = Filter B
- Display direction control (S/W) (36h)
  - X-Mirror control by MX (D7)
  - Y-Mirror control by MY (D6)
  - XY-Exchange control by MV (D5)

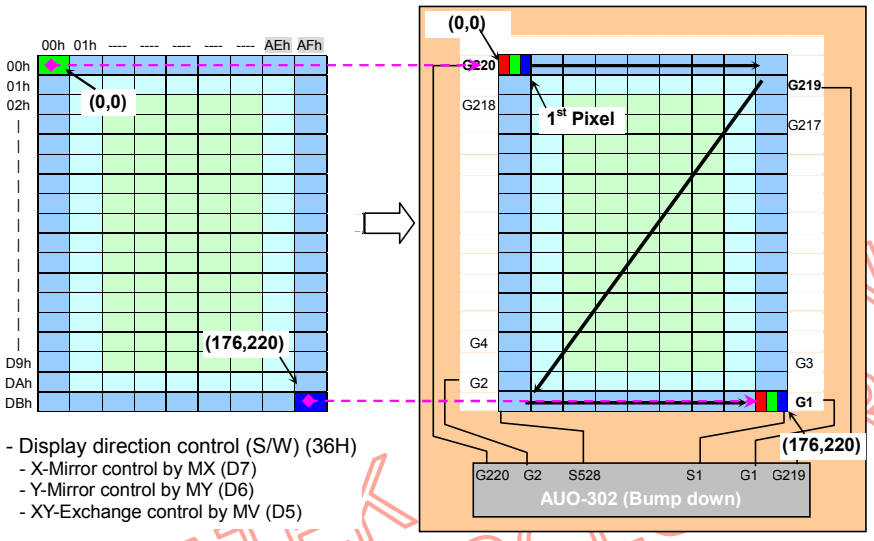


9.2 Application of connection with Different resolution (GRAM → Display)

Resolution 176RGB x 220
RAM size=176x 220 18-bits
Display size =176RGB x 220

1). Example for **SMX= '1' SMY='1'**

- Direction default setting (H/W)
  SMX = '1
  SMY = '1'
  SRGB = '1

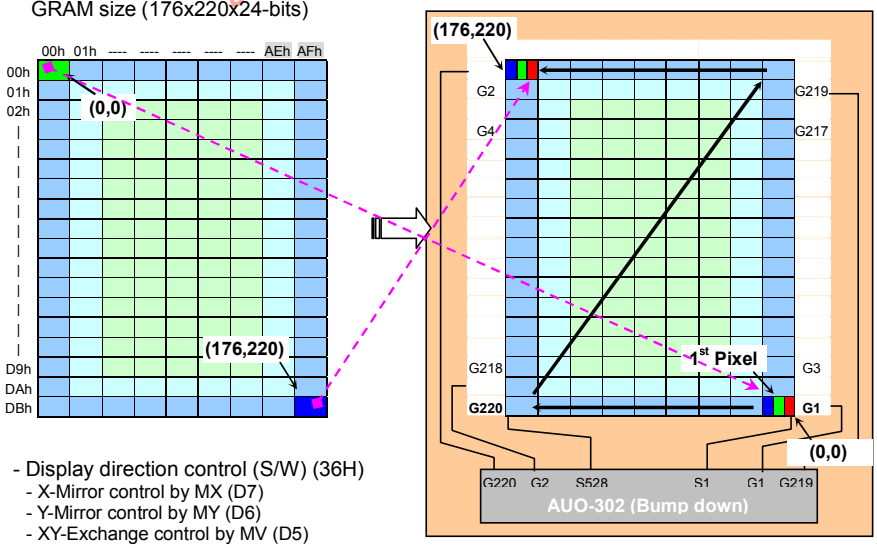


- Display direction control (S/W) (36H)
  - X-Mirror control by MX (D7)
  - Y-Mirror control by MY (D6)
  - XY-Exchange control by MV (D5)

2). Example for **SMX= '0' SMY='1'**

- Direction default setting (H/W)
  SMX = '0'
  SMY = '0'
  SRGB = '0'

GRAM size (176x220x24-bits)



- Display direction control (S/W) (36H)
  - X-Mirror control by MX (D7)
  - Y-Mirror control by MY (D6)
  - XY-Exchange control by MV (D5)

10 MicroProcessor Interface applications

10.1 MCU + SPI Interface Mode 1 (RCM1, RCM0 = '00', VSYNCOFF (ACH))

1. 8-bits data bus (IM1, IM0="00")

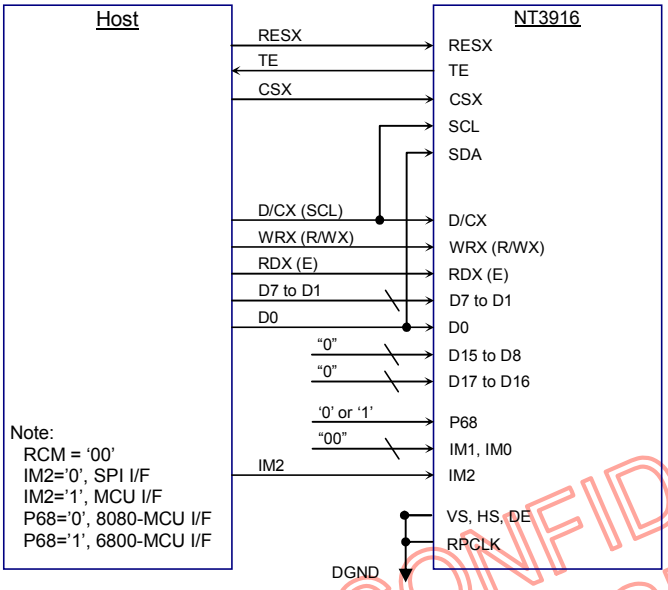


Fig. 10.1.1 MCU Interface for 8-bits data bus

2. 16-bits data bus (IM1, IM0="01")

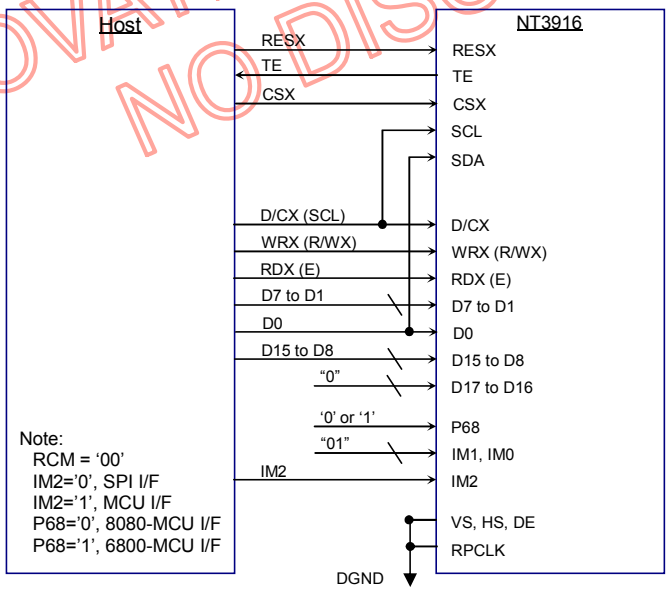


Fig. 10.1.2 MCU Interface for 16-bits data bus

3. 9-bits data bus (IM1, IM0=”10”)

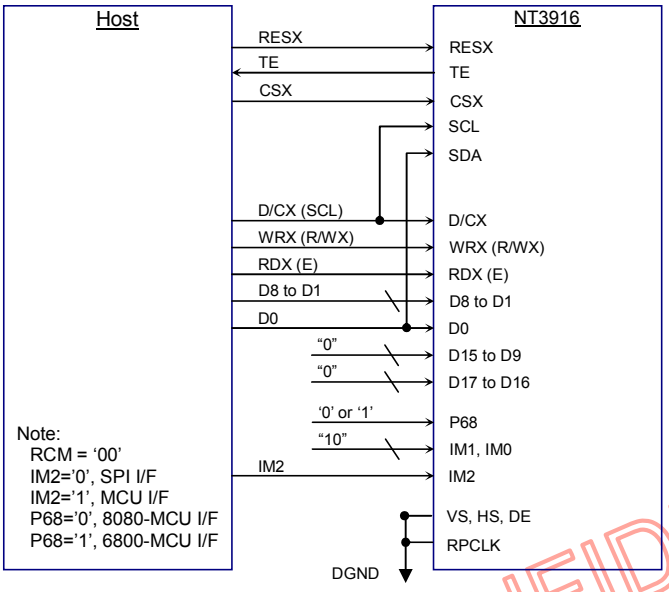


Fig. 10.1.3 MCU Interface for 9-bits data bus

4. 18-bits data bus (IM1, IM0=”11”)

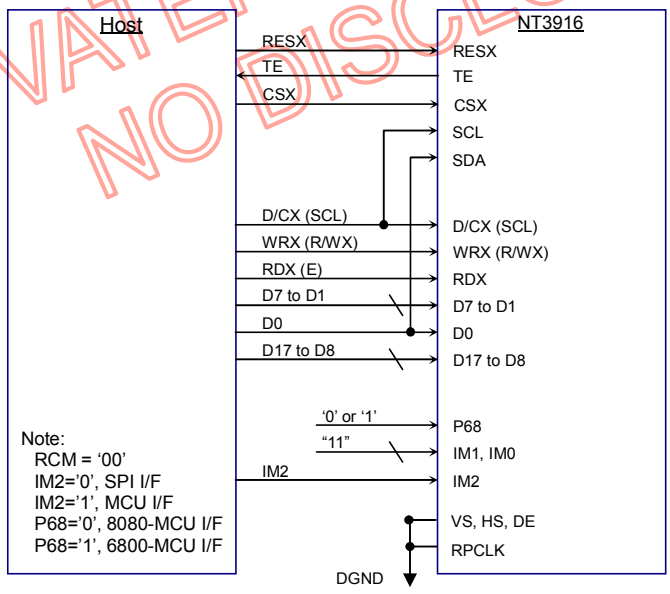


Fig. 10.1.4 MCU Interface for 18-bits data bus

10.2 MCU + SPI Interface mode 2 (RCM1, RCM0 =”01”, VSYNCOFF (ACH))

1. 8-bits data bus (IM1, IM0=”00”)

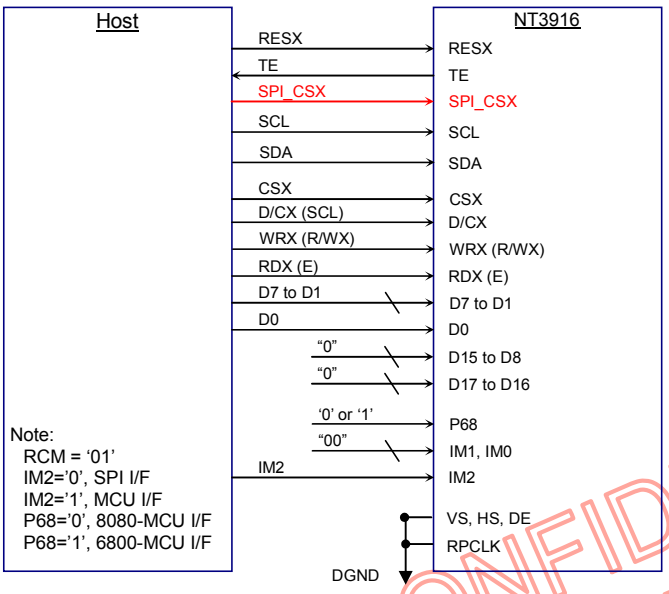


Fig. 10.2.1 MCU Interface for 8-bits data bus

2. 16-bits data bus (IM1, IM0=”01”)

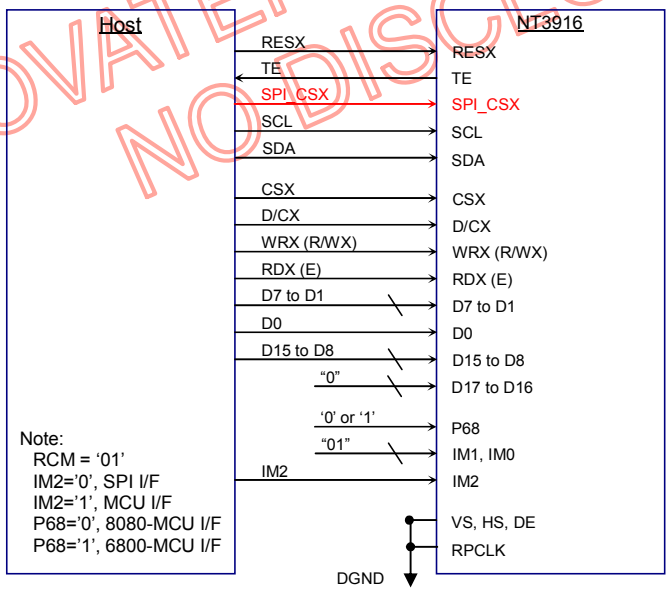


Fig. 10.2.2 MCU Interface for 16-bits data bus

3. 9-bits data bus (IM1, IM0=”10”)

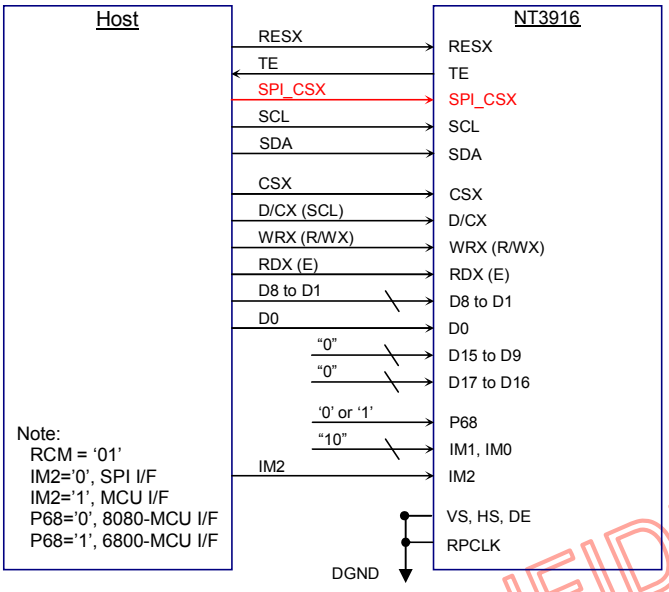


Fig. 10.2.3 MCU Interface for 9-bits data bus

4. 18-bits data bus (IM1, IM0=”11”)

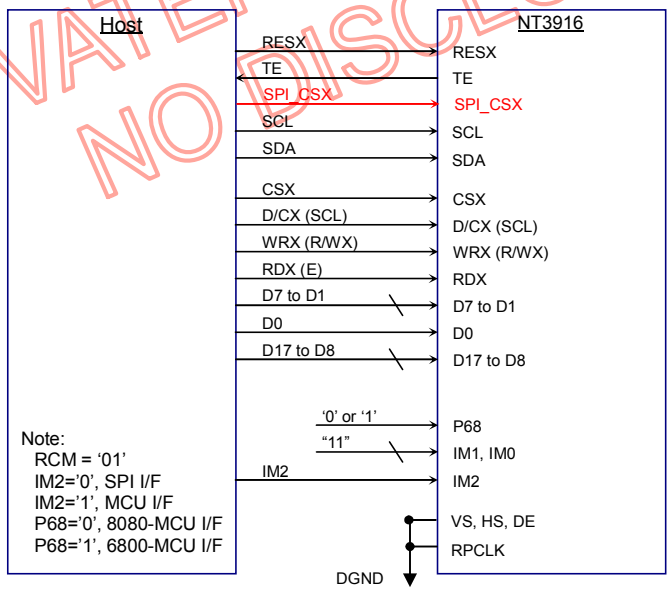


Fig. 10.2.4 MCU Interface for 18-bits data bus

10.3 MCU + SPI Interface mode 2 (RCM1, RCM0 =”01”, VSYNCON (ADH))

1. 8-bits data bus (IM1, IM0=”00”)

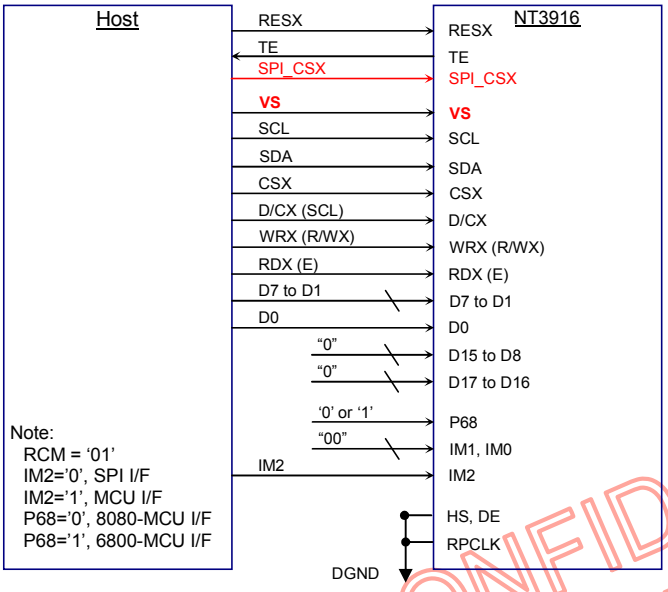


Fig. 10.3.1 VSYNC Interface for 8-bits data bus

2. 16-bits data bus (IM1, IM0=”01”)

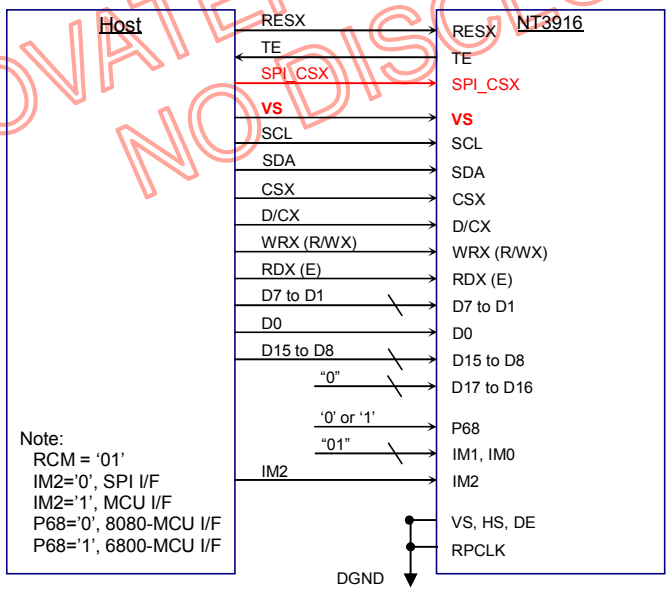


Fig. 10.3.2 VSYNC Interface for 16-bits data bus

3. 9-bits data bus (IM1, IM0=”10”)

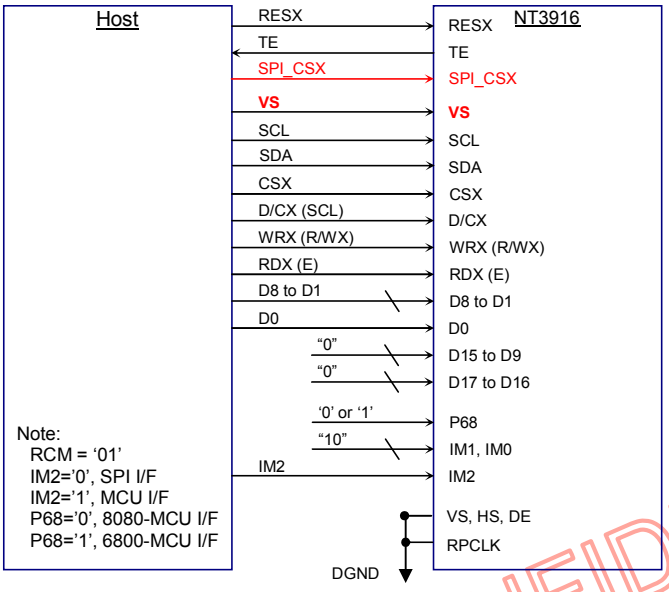


Fig. 10.3.3 VSYNC Interface for 9-bits data bus

4. 18-bits data bus (IM1, IM0=”11”)

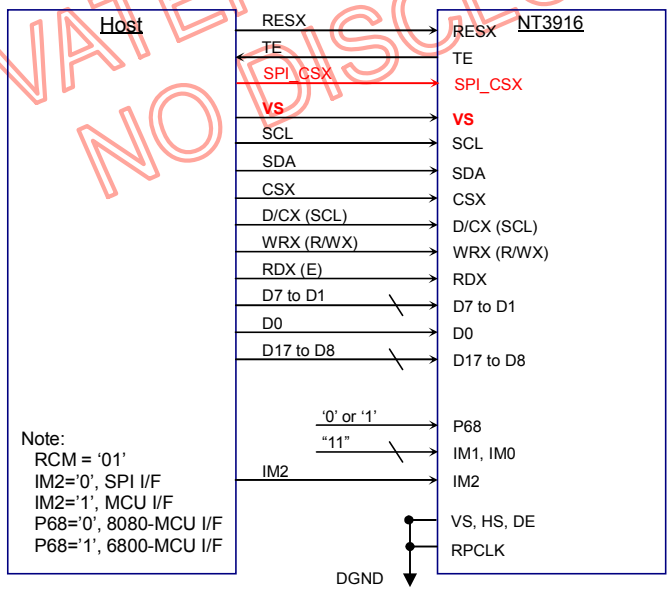


Fig. 10.3.4 VSYNC Interface for 18-bits data bus

10.4 RGB Interface (RCM = '1x')

1. RGBInterface for 6-bits Data Width

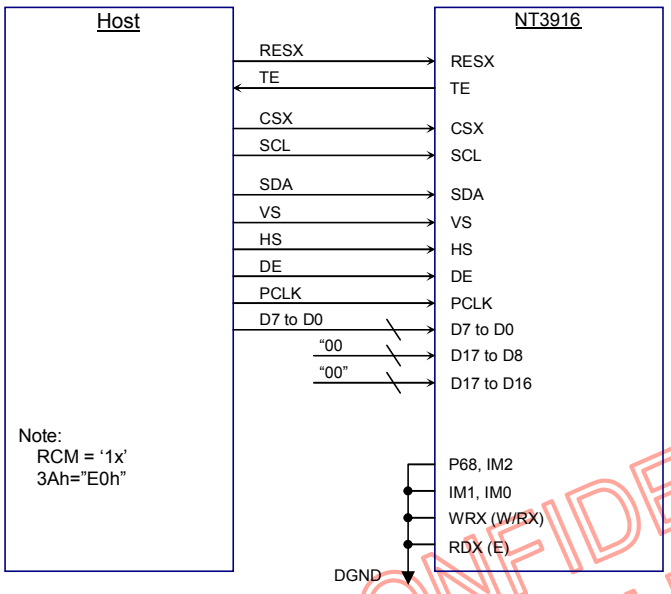


Fig. 10.4.1 RGB Interface for 8-bits data width

2. RGBInterface for 16-bits Data Width

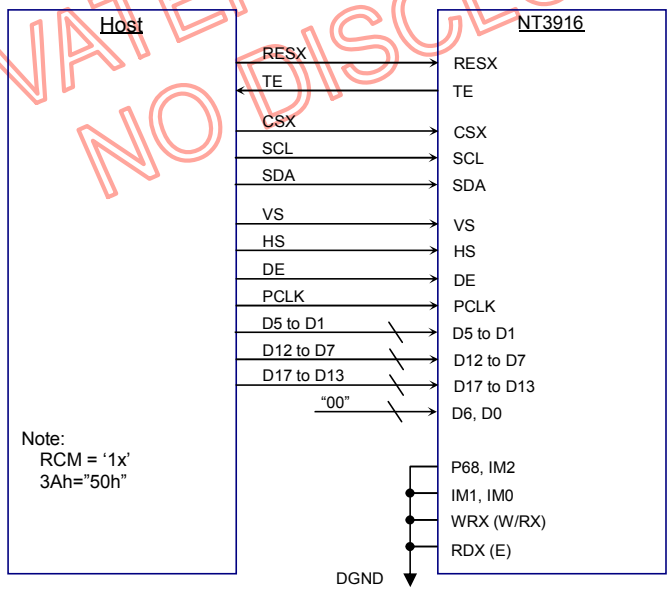


Fig. 10.4.2 RGB Interface for 16-bits data width

3. RGBInterface for 18-bits Data Width

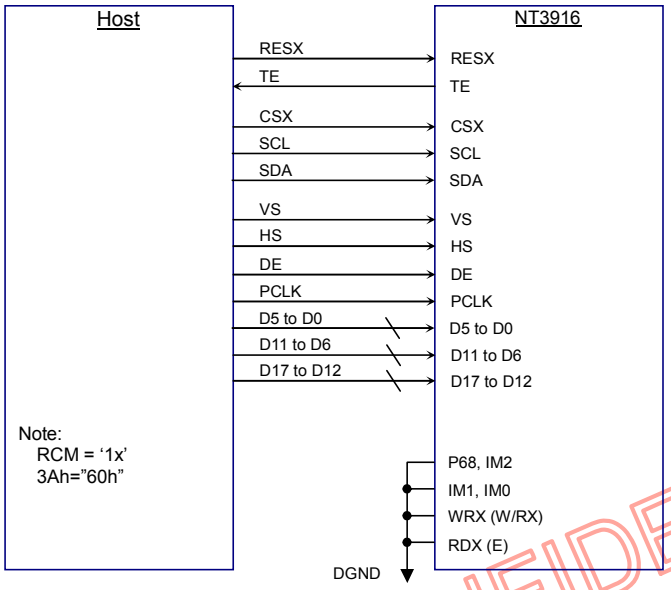


Fig. 10.4.3 RGB Interface for 18-bits data width

11 CHIP INFORMATION

-Chip Size= 18.65x1.05mm *(include of Scribe Line)*
-Chip Size can shrink Y-side

-Chip Thickness = 300um (Type)
-Bump height= 15um

11.1 Bump Information

11.1.1 Output Bump Dimension (Source/ Gate /Dummy)

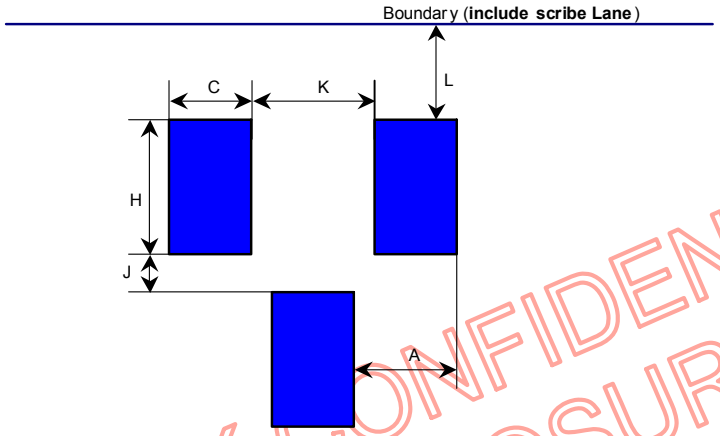


Fig 11.1.1 Output Bump Dimension

Item	Symbol	Size
Bump pitch	A	23 um
Bump width	C	21 um
Bump height	H	96 um
Bump gap1 (Vertical)	J	35 um
Bump gap2 (Horizontal)	K	25 um
Bump area	CxH	2016 um^2
Chip Boundary(include scribe Lane)	L	45~70 um

11.1.2 Input Bump Dimension

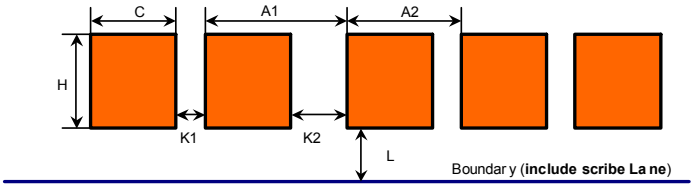


Fig 11.1.2 Input Bump Dimension

Item	Symbol	Size
Bump pitch 1	A1	64 um
Bump pitch 2	A2	80 um
Bump width	C	55 um
Bump height	H	96 um
Bump gap1	K1	9 um
Bump gap2	K2	25 um
Bump area	CxH	5280 um^2
Chip Boundary(include scribe Lane)	L	45~70 um

11.2 Alignment Mark Information

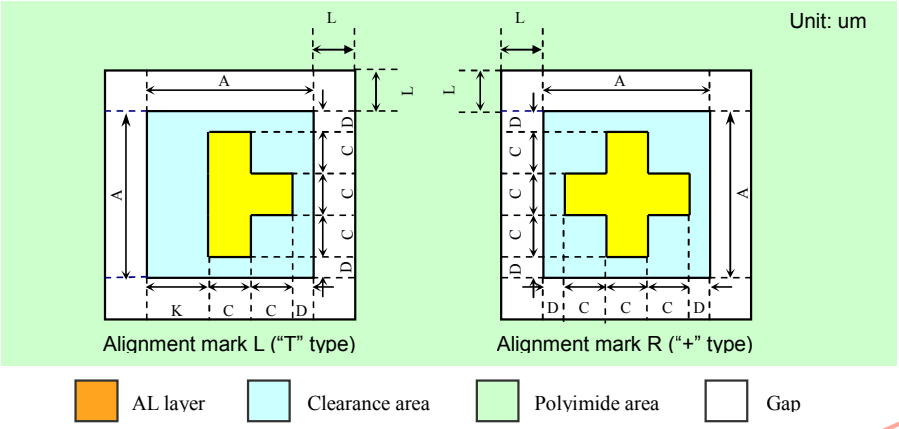


Fig. 11.2 IC Alignment Mark Dimension

Item	Symbol	Size
Alignment mark size	A	105um
Clearance gap 1	D	15um
Clearance gap 2	K	40um
Alignment mark width	C	25um
Alignment area	AxA	11025um2
Gap width	L	40~48um

11.3 Bump Location and Dimension

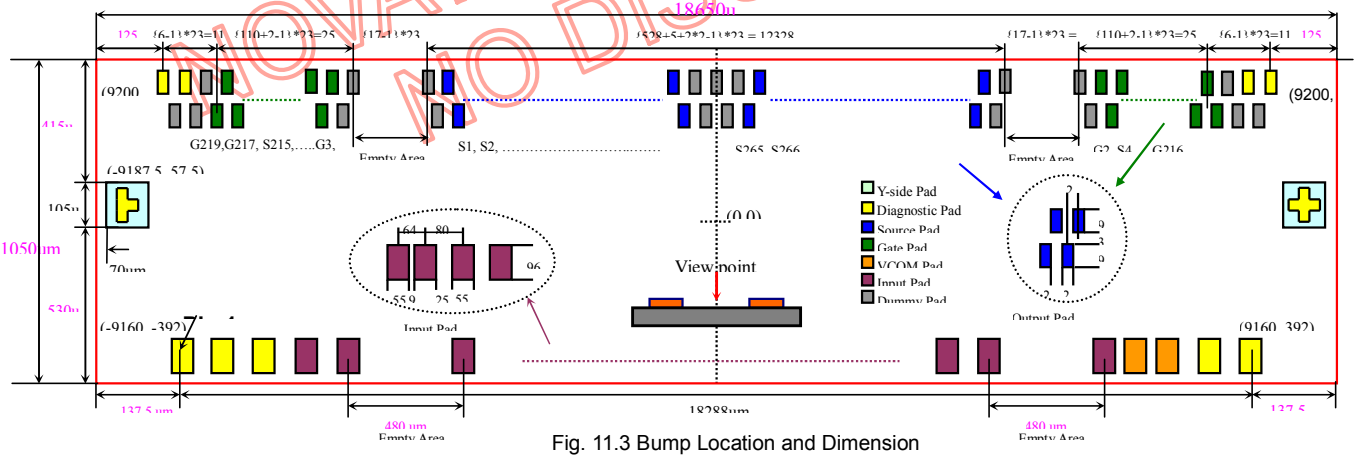


Fig. 11.3 Bump Location and Dimension

Note 1. Pad locations please follow above format.

Note 2. Die Size suggest 18.65mm x 1.05mm

*Note 3. Output Pad pitch is **23um**.*

Note 4. Input Pads name and order need to be discussed later.

12. Pin assignment and coordinate

No.	SPEC Pad	X	Y
1	PADA1	-9160	-392
2	PADB1	-9080	-392
3	PADA0	-9000	-392
4	Reserved	-8920	-392
5	Reserved	-8840	-392
6	EXTC	-8760	-392
7	VDDIO	-8680	-392
8	IM0	-8600	-392
9	IM1	-8520	-392
10	IM2	-8440	-392
11	P68	-8360	-392
12	DGNDO	-8280	-392
13	SPI_CSX	-8200	-392
14	4WSPI	-8120	-392
15	DUMMYA[3]	-8040	-392
16	VDDIO	-7960	-392
17	RCM0	-7880	-392
18	RCM1	-7800	-392
19	DGNDO	-7720	-392
20	SRGB	-7640	-392
21	SMX	-7560	-392
22	SMY	-7480	-392
23	VDDIO	-7400	-392
24	PREG	-7320	-392
25	RL	-7240	-392
26	TB	-7160	-392
27	SHUT	-7080	-392
28	IDM	-7000	-392
29	REV	-6920	-392
30	DGNDO	-6840	-392
31	GM1	-6760	-392
32	GM0	-6680	-392
33	VDDIO	-6600	-392
34	DGNDO	-6120	-392
35	LCM1	-6040	-392
36	LCM0	-5960	-392
37	VDDIO	-5880	-392
38	**TEST [1]**	-5800	-392
39	**TEST [2]**	-5720	-392
40	**TEST [3]**	-5640	-392
41	**TEST [4]**	-5560	-392
42	**TEST [5]**	-5480	-392
43	D17	-5400	-392
44	D17	-5336	-392
45	D16	-5256	-392
46	D16	-5192	-392
47	D15	-5112	-392
48	D15	-5048	-392
49	D14	-4968	-392
50	D14	-4904	-392
51	D13	-4824	-392
52	D13	-4760	-392
53	D12	-4680	-392
54	D12	-4616	-392
55	D11	-4536	-392
56	D11	-4472	-392
57	D10	-4392	-392
58	D10	-4328	-392
59	D9	-4248	-392
60	D9	-4184	-392
61	D8	-4104	-392
62	D8	-4040	-392
63	DGNDO	-3960	-392
64	DGNDO	-3896	-392
65	D7	-3816	-392
66	D7	-3752	-392
67	D6	-3672	-392
68	D6	-3608	-392
69	D5	-3528	-392
70	D5	-3464	-392
71	D4	-3384	-392
72	D4	-3320	-392
73	D3	-3240	-392
74	D3	-3176	-392
75	D2	-3096	-392
76	D2	-3032	-392
77	D1	-2952	-392
78	D1	-2888	-392
79	D0 (SDA)	-2808	-392
80	D0 (SDA)	-2744	-392
81	**TEST [6]**	-2664	-392
82	**TEST [7]**	-2584	-392
83	**TEST [8]**	-2504	-392
84	**TEST [9]**	-2424	-392
85	**TEST [10]**	-2344	-392
86	OSC	-2264	-392
87	TE	-2184	-392
88	CSX	-2104	-392
89	RDX (E)	-2024	-392
90	WRX (R/Wx)	-1944	-392
91	SDA	-1864	-392
92	**TEST [11]**	-1784	-392
93	**TEST [12]**	-1704	-392
94	**TEST [13]**	-1624	-392
95	RESX	-1544	-392
96	DGND	-1464	-392
97	D/CX (SCL)	-1384	-392
98	DGND	-1304	-392
99	SCL	-1224	-392
100	DGND	-1144	-392
101	PCLK	-1064	-392
102	DGND	-984	-392
103	DE	-904	-392
104	HS	-824	-392
105	VS	-744	-392
106	DUMMYA[4]	-664	-392
107	**TEST [14]**	-584	-392
108	**TEST [15]**	-504	-392
109	**TEST [16]**	-424	-392
110	**TEST [17]**	-344	-392
111	**TEST [18]**	-264	-392
112	DGND	-184	-392
113	DGND	-120	-392
114	DGND	-56	-392
115	DGND	8	-392
116	DGND	72	-392
117	DGND	136	-392
118	DGND	200	-392
119	DGND	264	-392
120	DGND	328	-392
121	DGND	392	-392
122	DGND	456	-392
123	DGND	520	-392
124	VCC	600	-392
125	VCC	664	-392
126	VCC	728	-392
127	VCC	792	-392
128	VCC	856	-392
129	VDDI	936	-392
130	VDDI	1000	-392
131	VDDI	1064	-392
132	VDDI	1128	-392
133	VDDI	1192	-392
134	VDDI	1256	-392
135	VDDI	1320	-392
136	VDDI	1384	-392
137	VDD	1464	-392
138	VDD	1528	-392
139	VDD	1592	-392
140	VDD	1656	-392

141	VDD	1720	-392
142	VDD	1784	-392
143	VDD	1848	-392
144	VDD	1912	-392
145	VDD	1976	-392
146	VDD	2040	-392
147	GVDD	2120	-392
148	GVDD	2184	-392
149	GVDD	2248	-392
150	GVDD	2312	-392
151	AGND	2392	-392
152	AGND	2456	-392
153	AGND	2520	-392
154	AGND	2584	-392
155	AGND	2648	-392
156	AGND	2712	-392
157	AGND	2776	-392
158	AGND	2840	-392
159	AGND	2904	-392
160	AGND	2968	-392
161	VREF	3048	-392
162	VREF	3112	-392
163	VREF	3176	-392
164	VREF	3240	-392
165	VREF	3304	-392
166	TEST [19]	3384	-392
167	TEST [20]	3464	-392
168	DUMMYB[1]	3544	-392
169	VcomH	3624	-392
170	VcomH	3688	-392
171	VcomH	3752	-392
172	VcomH	3816	-392
173	VcomL	3896	-392
174	VcomL	3960	-392
175	VcomL	4024	-392
176	VcomL	4088	-392
177	VCI1	4168	-392
178	VCI1	4232	-392
179	VCI1	4296	-392
180	VCI1	4360	-392
181	VCI1	4424	-392
182	AVDD	4504	-392
183	AVDD	4568	-392
184	AVDD	4632	-392
185	AVDD	4696	-392
186	AVDD	4760	-392
187	AVDD	4824	-392
188	C11+	4904	-392
189	C11+	4968	-392
190	C11+	5032	-392
191	C11+	5096	-392
192	C11-	5176	-392
193	C11-	5240	-392
194	C11-	5304	-392
195	C11-	5368	-392
196	C12+	5448	-392
197	C12+	5512	-392
198	C12+	5576	-392
199	C12+	5640	-392
200	C12-	5720	-392
201	C12-	5784	-392
202	C12-	5848	-392
203	C12-	5912	-392
204	AGND	5992	-392
205	AGND	6056	-392
206	AGND	6120	-392
207	AGND	6184	-392
208	AGND	6248	-392
209	VCL	6728	-392
210	VCL	6792	-392
211	VCL	6856	-392
212	C21+	6936	-392
213	C21+	7000	-392
214	C21+	7064	-392
215	C21-	7144	-392
216	C21-	7208	-392
217	C21-	7272	-392
218	C22+	7352	-392
219	C22+	7416	-392
220	C22+	7480	-392
221	C22-	7560	-392
222	C22-	7624	-392
223	C22-	7688	-392
224	C23+	7768	-392
225	C23+	7832	-392
226	C23+	7896	-392
227	C23-	7976	-392
228	C23-	8040	-392
229	C23-	8104	-392
230	VgL	8184	-392
231	VgL	8248	-392
232	VgL	8312	-392
233	VgH	8392	-392
234	VgH	8456	-392
235	VgH	8520	-392
236	PADB0	8600	-392
237	VCOM	8680	-392
238	VCOM	8744	-392
239	VCOM	8808	-392
240	VCOM	8872	-392
241	VCOM	8936	-392
242	VCOM	9000	-392
243	PADA2	9080	-392
244	PADB2	9160	-392
245	PADA3	9200	392
246	DUMMYA[5]	9177	261
247	PADB3	9154	392
248	DUMMYA[6]	9131	261
249	DUMMYA[7]	9108	392
250	G220	9085	261
251	G218	9062	392
252	G216	9039	261
253	G214	9016	392
254	G212	8993	261
255	G210	8970	392
256	G208	8947	261
257	G206	8924	392
258	G204	8901	261
259	G202	8878	392
260	G200	8855	261
261	G198	8832	392
262	G196	8809	261
263	G194	8786	392
264	G192	8763	261
265	G190	8740	392
266	G188	8717	261
267	G186	8694	392
268	G184	8671	261
269	G182	8648	392
270	G180	8625	261
271	G178	8602	392
272	G176	8579	261
273	G174	8556	392
274	G172	8533	261
275	G170	8510	392
276	G168	8487	261
277	G166	8464	392
278	G164	8441	261
279	G162	8418	392
280	G160	8395	261
281	G158	8372	392
282	G156	8349	261
283	G154	8326	392
284	G152	8303	261

285	G150	8280	392
286	G148	8257	261
287	G146	8234	392
288	G144	8211	261
289	G142	8188	392
290	G140	8165	261
291	G138	8142	392
292	G136	8119	261
293	G134	8096	392
294	G132	8073	261
295	G130	8050	392
296	G128	8027	261
297	G126	8004	392
298	G124	7981	261
299	G122	7958	392
300	G120	7935	261
301	G118	7912	392
302	G116	7889	261
303	G114	7866	392
304	G112	7843	261
305	G110	7820	392
306	G108	7797	261
307	G106	7774	392
308	G104	7751	261
309	G102	7728	392
310	G100	7705	261
311	G98	7682	392
312	G96	7659	261
313	G94	7636	392
314	G92	7613	261
315	G90	7590	392
316	G88	7567	261
317	G86	7544	392
318	G84	7521	261
319	G82	7498	392
320	G80	7475	261
321	G78	7452	392
322	G76	7429	261
323	G74	7406	392
324	G72	7383	261
325	G70	7360	392
326	G68	7337	261
327	G66	7314	392
328	G64	7291	261
329	G62	7268	392
330	G60	7245	261
331	G58	7222	392
332	G56	7199	261
333	G54	7176	392
334	G52	7153	261
335	G50	7130	392
336	G48	7107	261
337	G46	7084	392
338	G44	7061	261
339	G42	7038	392
340	G40	7015	261
341	G38	6992	392
342	G36	6969	261
343	G34	6946	392
344	G32	6923	261
345	G30	6900	392
346	G28	6877	261
347	G26	6854	392
348	G24	6831	261
349	G22	6808	392
350	G20	6785	261
351	G18	6762	392
352	G16	6739	261
353	G14	6716	392
354	G12	6693	261
355	G10	6670	392
356	G8	6647	261
357	G6	6624	392
358	G4	6601	261
359	G2	6578	392
360	DUMMYA[8]	6555	261
361	DUMMYA[9]	6532	392
362	DUMMYA[10]	6164	392
363	DUMMYA[11]	6141	261
364	S528	6118	392
365	S527	6095	261
366	S526	6072	392
367	S525	6049	261
368	S524	6026	392
369	S523	6003	261
370	S522	5980	392
371	S521	5957	261
372	S520	5934	392
373	S519	5911	261
374	S518	5888	392
375	S517	5865	261
376	S516	5842	392
377	S515	5819	261
378	S514	5796	392
379	S513	5773	261
380	S512	5750	392
381	S511	5727	261
382	S510	5704	392
383	S509	5681	261
384	S508	5658	392
385	S507	5635	261
386	S506	5612	392
387	S505	5589	261
388	S504	5566	392
389	S503	5543	261
390	S502	5520	392
391	S501	5497	261
392	S500	5474	392
393	S499	5451	261
394	S498	5428	392
395	S497	5405	261
396	S496	5382	392
397	S495	5359	261
398	S494	5336	392
399	S493	5313	261
400	S492	5290	392
401	S491	5267	261
402	S490	5244	392
403	S489	5221	261
404	S488	5198	392
405	S487	5175	261
406	S486	5152	392
407	S485	5129	261
408	S484	5106	392
409	S483	5083	261
410	S482	5060	392
411	S481	5037	261
412	S480	5014	392
413	S479	4991	261
414	S478	4968	392
415	S477	4945	261
416	S476	4922	392
417	S475	4899	261
418	S474	4876	392
419	S473	4853	261
420	S472	4830	392
421	S471	4807	261
422	S470	4784	392
423	S469	4761	261
424	S468	4738	392
425	S467	4715	261
426	S466	4692	392
427	S465	4669	261
428	S464	4646	392

429	S463	4623	261
430	S462	4600	392
431	S461	4577	261
432	S460	4554	392
433	S459	4531	261
434	S458	4508	392
435	S457	4485	261
436	S456	4462	392
437	S455	4439	261
438	S454	4416	392
439	S453	4393	261
440	S452	4370	392
441	S451	4347	261
442	S450	4324	392
443	S449	4301	261
444	S448	4278	392
445	S447	4255	261
446	S446	4232	392
447	S445	4209	261
448	S444	4186	392
449	S443	4163	261
450	S442	4140	392
451	S441	4117	261
452	S440	4094	392
453	S439	4071	261
454	S438	4048	392
455	S437	4025	261
456	S436	4002	392
457	S435	3979	261
458	S434	3956	392
459	S433	3933	261
460	S432	3910	392
461	S431	3887	261
462	S430	3864	392
463	S429	3841	261
464	S428	3818	392
465	S427	3795	261
466	S426	3772	392
467	S425	3749	261
468	S424	3726	392
469	S423	3703	261
470	S422	3680	392
471	S421	3657	261
472	S420	3634	392
473	S419	3611	261
474	S418	3588	392
475	S417	3565	261
476	S416	3542	392
477	S415	3519	261
478	S414	3496	392
479	S413	3473	261
480	S412	3450	392
481	S411	3427	261
482	S410	3404	392
483	S409	3381	261
484	S408	3358	392
485	S407	3335	261
486	S406	3312	392
487	S405	3289	261
488	S404	3266	392
489	S403	3243	261
490	S402	3220	392
491	S401	3197	261
492	S400	3174	392
493	S399	3151	261
494	S398	3128	392
495	S397	3105	261
496	S396	3082	392
497	S395	3059	261
498	S394	3036	392
499	S393	3013	261
500	S392	2990	392
501	S391	2967	261
502	S390	2944	392
503	S389	2921	261
504	S388	2898	392
505	S387	2875	261
506	S386	2852	392
507	S385	2829	261
508	S384	2806	392
509	S383	2783	261
510	S382	2760	392
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514	S378	2668	392
515	S377	2645	261
516	S376	2622	392
517	S375	2599	261
518	S374	2576	392
519	S373	2553	261
520	S372	2530	392
521	S371	2507	261
522	S370	2484	392
523	S369	2461	261
524	S368	2438	392
525	S367	2415	261
526	S366	2392	392
527	S365	2369	261
528	S364	2346	392
529	S363	2323	261
530	S362	2300	392
531	S361	2277	261
532	S360	2254	392
533	S359	2231	261
534	S358	2208	392
535	S357	2185	261
536	S356	2162	392
537	S355	2139	261
538	S354	2116	392
539	S353	2093	261
540	S352	2070	392
541	S351	2047	261
542	S350	2024	392
543	S349	2001	261
544	S348	1978	392
545	S347	1955	261
546	S346	1932	392
547	S345	1909	261
548	S344	1886	392
549	S343	1863	261
550	S342	1840	392
551	S341	1817	261
552	S340	1794	392
553	S339	1771	261
554	S338	1748	392
555	S337	1725	261
556	S336	1702	392
557	S335	1679	261
558	S334	1656	392
559	S333	1633	261
560	S332	1610	392
561	S331	1587	261
562	S330	1564	392
563	S329	1541	261
564	S328	1518	392
565	S327	1495	261
566	S326	1472	392
567	S325	1449	261
568	S324	1426	392
569	S323	1403	261
570	S322	1380	392
571	S321	1357	261
572	S320	1334	392

573	S319	1311	261
574	S318	1288	392
575	S317	1265	261
576	S316	1242	392
577	S315	1219	261
578	S314	1196	392
579	S313	1173	261
580	S312	1150	392
581	S311	1127	261
582	S310	1104	392
583	S309	1081	261
584	S308	1058	392
585	S307	1035	261
586	S306	1012	392
587	S305	989	261
588	S304	966	392
589	S303	943	261
590	S302	920	392
591	S301	897	261
592	S300	874	392
593	S299	851	261
594	S298	828	392
595	S297	805	261
596	S296	782	392
597	S295	759	261
598	S294	736	392
599	S293	713	261
600	S292	690	392
601	S291	667	261
602	S290	644	392
603	S289	621	261
604	S288	598	392
605	S287	575	261
606	S286	552	392
607	S285	529	261
608	S284	506	392
609	S283	483	261
610	S282	460	392
611	S281	437	261
612	S280	414	392
613	S279	391	261
614	S278	368	392
615	S277	345	261
616	S276	322	392
617	S275	299	261
618	S274	276	392
619	S273	253	261
620	S272	230	392

621	S271	207	261
622	S270	184	392
623	S269	161	261
624	S268	138	392
625	S267	115	261
626	S266	92	392
627	S265	69	261
628	DUMMYA[12]	46	392
629	DUMMYA[13]	23	261
630	DUMMYA[14]	0	392
631	DUMMYA[15]	-23	261
632	DUMMYA[16]	-46	392
633	S264	-69	261
634	S263	-92	392
635	S262	-115	261
636	S261	-138	392
637	S260	-161	261
638	S259	-184	392
639	S258	-207	261
640	S257	-230	392
641	S256	-253	261
642	S255	-276	392
643	S254	-299	261
644	S253	-322	392
645	S252	-345	261
646	S251	-368	392
647	S250	-391	261
648	S249	-414	392
649	S248	-437	261
650	S247	-460	392
651	S246	-483	261
652	S245	-506	392
653	S244	-529	261
654	S243	-552	392
655	S242	-575	261
656	S241	-598	392
657	S240	-621	261
658	S239	-644	392
659	S238	-667	261
660	S237	-690	392
661	S236	-713	261
662	S235	-736	392
663	S234	-759	261
664	S233	-782	392
665	S232	-805	261
666	S231	-828	392
667	S230	-851	261
668	S229	-874	392

669	S228	-897	261
670	S227	-920	392
671	S226	-943	261
672	S225	-966	392
673	S224	-989	261
674	S223	-1012	392
675	S222	-1035	261
676	S221	-1058	392
677	S220	-1081	261
678	S219	-1104	392
679	S218	-1127	261
680	S217	-1150	392
681	S216	-1173	261
682	S215	-1196	392
683	S214	-1219	261
684	S213	-1242	392
685	S212	-1265	261
686	S211	-1288	392
687	S210	-1311	261
688	S209	-1334	392
689	S208	-1357	261
690	S207	-1380	392
691	S206	-1403	261
692	S205	-1426	392
693	S204	-1449	261
694	S203	-1472	392
695	S202	-1495	261
696	S201	-1518	392
697	S200	-1541	261
698	S199	-1564	392
699	S198	-1587	261
700	S197	-1610	392
701	S196	-1633	261
702	S195	-1656	392
703	S194	-1679	261
704	S193	-1702	392
705	S192	-1725	261
706	S191	-1748	392
707	S190	-1771	261
708	S189	-1794	392
709	S188	-1817	261
710	S187	-1840	392
711	S186	-1863	261
712	S185	-1886	392
713	S184	-1909	261
714	S183	-1932	392
715	S182	-1955	261
716	S181	-1978	392

717	S180	-2001	261
718	S179	-2024	392
719	S178	-2047	261
720	S177	-2070	392
721	S176	-2093	261
722	S175	-2116	392
723	S174	-2139	261
724	S173	-2162	392
725	S172	-2185	261
726	S171	-2208	392
727	S170	-2231	261
728	S169	-2254	392
729	S168	-2277	261
730	S167	-2300	392
731	S166	-2323	261
732	S165	-2346	392
733	S164	-2369	261
734	S163	-2392	392
735	S162	-2415	261
736	S161	-2438	392
737	S160	-2461	261
738	S159	-2484	392
739	S158	-2507	261
740	S157	-2530	392
741	S156	-2553	261
742	S155	-2576	392
743	S154	-2599	261
744	S153	-2622	392
745	S152	-2645	261
746	S151	-2668	392
747	S150	-2691	261
748	S149	-2714	392
749	S148	-2737	261
750	S147	-2760	392
751	S146	-2783	261
752	S145	-2806	392
753	S144	-2829	261
754	S143	-2852	392
755	S142	-2875	261
756	S141	-2898	392
757	S140	-2921	261
758	S139	-2944	392
759	S138	-2967	261
760	S137	-2990	392
761	S136	-3013	261
762	S135	-3036	392
763	S134	-3059	261
764	S133	-3082	392
765	S132	-3105	261
766	S131	-3128	392
767	S130	-3151	261
768	S129	-3174	392
769	S128	-3197	261
770	S127	-3220	392
771	S126	-3243	261
772	S125	-3266	392
773	S124	-3289	261
774	S123	-3312	392
775	S122	-3335	261
776	S121	-3358	392
777	S120	-3381	261
778	S119	-3404	392
779	S118	-3427	261
780	S117	-3450	392
781	S116	-3473	261
782	S115	-3496	392
783	S114	-3519	261
784	S113	-3542	392
785	S112	-3565	261
786	S111	-3588	392
787	S110	-3611	261
788	S109	-3634	392
789	S108	-3657	261
790	S107	-3680	392
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792	S105	-3726	392
793	S104	-3749	261
794	S103	-3772	392
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796	S101	-3818	392
797	S100	-3841	261
798	S99	-3864	392
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802	S95	-3956	392
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806	S91	-4048	392
807	S90	-4071	261
808	S89	-4094	392
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810	S87	-4140	392
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817	S80	-4301	261
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820	S77	-4370	392
821	S76	-4393	261
822	S75	-4416	392
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854	S43	-5152	392
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917	G33	-6946	392
918	G35	-6969	261
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922	G43	-7061	261
923	G45	-7084	392
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