1. Abstract

This document describes the difference between BK2423 chip and BK2421. The BK2423 chip is the upgrade version of BK2421. The BK2423 additional 250Kbps air rate supported, Compared with BK2421, the receive sensitivity of BK2423 is improved about 2dB, meanwhile the transmitting power decreased 2dB. In addition, the BK2423 is downward compatible with BK2421.

INHAOS Product list:

No.	Module Type	BK2421	BK2423	Remark
1	SPI interface Module	RF-2400P RF-2400W RF-2400-V03 RF-2400-NANO	RF-2423	RF-2423 support both SMD and DIP connector
2	RF Module with C8051F330 MCU	RF-2410M	RF-2423M	
3	USB RF Module (C8051F321 MCU)	RF-2410U	RF-2423U	RF-2423U add two LED

2. The Difference between BK2421 and BK2423

This section describes the detail difference between BK2423 and BK2421. There are two case here:

(1).Differences must be considered in design;

(2).Differences usually no need to consider in design.

Differences must be considered in design

No.	The differences must be considered in design	BK2421	BK2423
1	Bank Register Count	Bank1,Bank0	Bank1,Bank0
2	Power On Initialize	Two Register must be initialized, the detail steps as follow: (1) Read the Bank state Bank0_REG7[7]=RBANK＝(0:Bank0;1:Bank1)， If the current bank is Bank0，then switch the bank to bank1 using ACTIVATE + 0x53, if the current bank is already Bank1, jump to step(2) directly. (2) Initialize registers of Bank1, the value of Bank1 registers, please reference the datasheet of BK2421.	It's not necessary to initialize the Bank1, except for the special needs. In that case, user can follow the Bank1 initialization steps of BK2421.

		Please Note: The byte order of REG0 to REG8 in Bank1 is: High byte first, then low byte; and MSB first in each byte. The byte order of REG9 to REG14 in Bank1 is: Low byte first, then high byte; and MSB first in each byte. The byte order of the registers in Bank0 is: Low byte first, then high byte; and MSB first in each byte. (3) Switch to Bank0 using SPI command ACTIVATE + 0x53.	
3	Air data rate	Supports 1Mbps/2Mbps	Supports 1Mbps/2Mbps/250Kbps
5	Bank0_REG6[4]=PLL_LOCK Register	This bit is not used. The single carrier transmit is controlled by Bank1_REG4=0xD9BE8621。	**This bit must set to 0, when application software needs compatible with both BK2423 and BK2421.**

(Form-01)

Differences usually do not need to consider in design:

No.	Differences usually do not need to consider in design	BK2421	BK2423
2	After CE is 0, RX_DR interrupt will be cleared.	After CE set low, RX_DR interrupt will be auto clear, so you should handle interrupt before CE pin is low.	After CE is 0, interrupt will not clear
3	Interrupt trigger time of PTX,PRX	When the PRX send ACK with payload, （1）.the PRX end: RX_DR and TX_DS set to 1 in the same time; （2）.the PTX end: TX_DS will be set high first. RX_DR than TX_DS delay 2~3us	When the PRX send ACK with payload, （1）.the PRX end: TX_DS set to 1 delay one packet than RX_DR （2）.the PTX end: same with the BK2421.
5	CD Detection	There are Control switch and contrast threshold. Set contrast threshold in BANK1_REG5[29:26]. 0: -97dBm 15:-67dBm step 2dB. When detected continuously 128us interference signal is greater than the set threshold ,Bank0_REG9[0] will be set high , and will keep to high until reading the CD value. If you do not need CD function , please turn it OFF to save power approximately 1mA (The CD function default is OFF)	There are Control switch and contrast threshold. Set contrast threshold in BANK1_REG5[29:26], the value is very different with BK2421. but detection method is the same as BK2421

6	TX power	The output power of eight levels. The maximum value is 5dBm, The minimum value is -40dBm.	The output power of eight levels. The maximum value is 3dBm, The minimum value is -40dBm.
7	PLL Locking time setting: Bank1_REG12 [26:24]	The default value is 120us, Bank1_REG12[26:24]= 000; Bank1_REG12=0x00731200	The default value is 130us Bank1_REG12[26:24]= 101; Bank1_REG12=0x05731200,

(Form-02)

3. How to get high transmission power mode in BK2423

If you need set the BK2423 TX power greater than 3dBm, you can modif BANK0 and BANK1 register, in this application, you need to add RF filter to meet the FCC standards. If you need set the TX power greater than 15dBm, you should add external power amplifier.

The BK2423 work in High output power and high current mode by modifying the Bank register

Register	High power Mode	Default value	comment
RF_PWR[2]＝Bank1_REG4[20] RF_PWR[1:0]＝Bank0_REG6[2:1]	0x07	0x06	
IctrlPA[0]= Bank1_REG4[9]	0x00	0x01	
txIctrl[2:0]=Bank1_REG4[29:27]	0x07	0x03	
Rvco_tx[2:0]=Bank1_REG3[31:29]	0x07	0x04	
Bank0_REG6 value	0x0F	0x0D	
Bank1_REG3 value	0xF9003941	0x99003941	
Bank1_REG4 value	0xF9BE840B	0xD9BE860B	
Output power	>3dBm	0dBm	

(Form-03)

4. How to get the lowest power consumption in power down mode?

Please set CSN high and set CE low. If there are pull-high resistors in MCU, please set CLK and MOSI high. If there are no pull-high resistors in MCU, please set CLK and MOSI low.

5. Air Rate Contrast table of BK2423 and BK2421

The BK2423 add 250Kbps air rate supported. Air rate of BK3423 can be controlled by Bank0_Reg06[3,5] = RF_DR_HIGH,RF_DR_LOW. Only used Bank0_Reg06[3] bit in BK2421.

Bank0_Reg6[5]=RF_DR_LOW	Bank0_Reg6[3]=RF_DR_HIGH	BK2421_Rate	BK2423_Rate
0	0	1Mbps	1Mbps
0/1	1	2Mbps	2Mbps
1	0	*	250Kbps

(Form-04)

6. Output power contrast table of BK2423 and BK2421

Note that the default setting of Bank1_REG4 is 0xD9BE860B. Output power can be controlled by RF_PWR[2:0]. The highest bit RF_PWR[2] is Bank1_Reg4[20]; and the other 2 bits RF_PWR[1:0] are Bank0_Reg6[2:1]. Output power table is as below:

RF_PWR[2] ＝ Bank1_REG4[20]	RF_PWR[1:0]＝ Bank0_REG6[2:1]	BK2423 Output power(dBm)	BK2421 Output power(dBm)	Current（mA）
1	11	3	5	23
1	10	-2(default)	0(默认)	17
1	01	-7	-5	15
1	00	-15	-10	13
0	11	-25	-25	12
0	10	-30	-30	11
0	01	-30	-30	11
0	00	-40	-40	11

(Form-05)

7. How to control receive sensitivity of the BK2423 in BANK1_REG4[21]=RX_SEN?

It add function of receive sensitivity in the BK2423 . Receive sensitivity will improved when set RX_SEN is 1. Receive sensitivity is the same as BK2421 when RX_SEN is 0.

Air Rate	Sensitivity (RX_SEN = 0)	Sensitivity (RX_SEN = 1)	Remark
250Kbps	-91dBm	-97dBm	
1Mbps	-88dBm-	-90dBm	
2Mbps	-85dBm	-87dBm	

8. RSSI Measurement

CD detection value of BK2423 is different from BK2421, it is not linear relationship with input power, especially when RX_SEN is 1, many point can not detect the CD value. Note 250Kbps and 1Mbps CD value is same.

CD value in 250Kbps/1Mbps air rate is as below:

Bank1_REG4[21]=RX_SEN=0	Bank1_REG4[21]=RX_SEN=1	Bank1_REG5[26:29]=RSSI_TH
NA	NA	0x00
-105dBm	NA	0x02
-101dBm	NA	0x01
-98dBm	NA	0x03
-95dBm	NA	0x08
-93dBm	NA	0x0A
-91dBm	NA	0x09 (Default)
-88dBm	NA	0x0B
-86dBm	NA	0x04
-83dBm	-106dBm	0x06
-81dBm	-102dBm	0x05
-78dBm	-99dBm	0x07
-76dBm	-97dBm	0x0C
-74dBm	-95dBm	0x0E
-71dBm	-93dBm	0x0D
-69dBm	-90dBm	0x0F

(Form-08)

CD threshold in 2Mbps air rate is as below:

Step	Threshold (RX_SEN = 0)	Threshold (RX_SEN = 1)	RSSI_TH
0	-100dBm	NA	0x00
1	-96dBm	NA	0x02
2	-94dBm	NA	0x01
3	-91dBm	NA	0x03
4	-88dBm	NA	0x08
5	-86dBm	NA	0x0A
6	-84dBm	NA	0x09(default)
7	-82dBm	-108dBm	0x0B
8	-79dBm	-99dBm	0x04
9	-77dBm	-97dBm	0x06
10	-74dBm	-94dBm	0x05
11	-72dBm	-92dBm	0x07

12	-70dBm	-90dBm	0x0C
13	-67dBm	-88dBm	0x0E
14	-65dBm	-86dBm	0x0D
15	-62dBm	-83dBm	0x0F

(Form-09)

9. How to operate FEATRUE register Bank0_REG29 and Bank0_REG7=RBANK

Before read/write these registers, you should sent command ACTIVATE(+0x73 +0x53) to activate the chip. User should read this register before activate. you can send activate command only when read result is 0. After activate you can write the value into the register. If it's activated already. It will change to un-activated mode. In un-activated mode, the return value of read operation is 0.

10. How to communicate between BK2421 and BK2423

If you want to BK2423 compatible with BK2421,you should set PLL locking time of BK2423 for 130us(Bank1_REG12= 0x00127305); If you want to BK2423 compatible with BK2421,you should set PLL locking time of BK2423 for 120us(Bank1_REG12= 0x00127300);

The default value of Register Bank0_REG6[4] is 1 in BK2421. When Register Bank0_REG6[4] is 1, It will trigger PLL LOCK test mode of BK2423. So the initial value of BK2421 will let BK2423 into PLL LOCK test mode. If you want software of BK2421 compatible with BK2423,you should set Bank0_REG6[4] for 1.

10. Reference Document

1) "BK2423 Datasheet v2.0"
2) "BK2423 Application Notes v2.0_en"
3) "BK2421 Datasheet v2.0"

Declare

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